M4K1553Px

MIL-STD-1553
Test and Simulation Module for the EXC-4000 Family of Carrier Boards

User's Manual

EXCALIBUR SYSTEMS

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1 Introduction

Chapter 1 provides an overview of the *M4K1553Px* avionics communication module. The following topics are covered:

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1.1 Overview

The *M4K1553Px* is an intelligent, MIL-STD-1553 interface module for the multimode, multiprotocol, Excalibur 4000 family of carrier boards. The *M4K1553Px* provides a complete solution for developing and testing 1553 interfaces and performing system simulation of the MIL-STD-1553 bus. The module handles all standard variations of the MIL-STD-1553 protocol. Each module of the *M4K1553Px* contains 64K bytes of dual-port RAM for Data Blocks, control registers, and Look-up tables. All Data Blocks and control registers are memory mapped, and may be accessed in real time.

Each of the independent dual redundant *M4K1553Px* modules may be programmed to operate in one of three modes of operation: Remote Terminal, Bus Controller/Concurrent-RT, and Bus Monitor. In addition, modules 1 and 3 can be programmed to operate as Concurrent monitors, to modules 0 and 2 respectively.

The *M4K1553Px* comes complete with Windows software, a C-driver software library including source code, and 1553 mating connectors with plastic hoods.

The *M4K1553Px*-E option is an extended temperature (-40° – +85°C) version of the module.

1.1.1 *M4K1553Px* Module Feature

- Independent 1553 dual-redundant module
- Real-time operation
- Operates as RT, BC/Concurrent-RT or Triggerable Bus Monitor
- Handles 4 μsec. intermessage gap times in all modes
- Multiple protocol capability (i.e. 1553A/B, F-16)
- Multiple-RT simulation (up to 32 Remote Terminals
- Extended Temperature range available – -40º–+85ºC
- Programmable broadcast mode
- Multi-mode triggerable Monitor
- Extensive interrupt features
- Error injection capability:
  - Word Count (+/–3 words)
  - Incorrect sync
  - Incorrect RT address
  - Non-contiguous data

PMx Option

Concurrent Monitor in RT and BC/RT modes

1760 Option

Checksum error detection
Checksum error injection

See Chapter 8: **Ordering Information**, for the exact part numbers.

Examples of user selectable parameters are:

- The user can select whether an RT will return a Status word in the event a message containing a Data Word error is received by the RT.
- Selectable broadcast mode
- Variable response time
- Select mode code subaddress (00000, 11111, or both)
- 1553A RT timing
- Each bit in the 1553 Status word can be defined by the user

The M4K1553P*x* has three modes of operation:

- Multiple Remote Terminal (RT) mode (up to 32 RTs)
- BC with Concurrent RT operation (up to 32 RTs)
- Triggerable Monitor mode

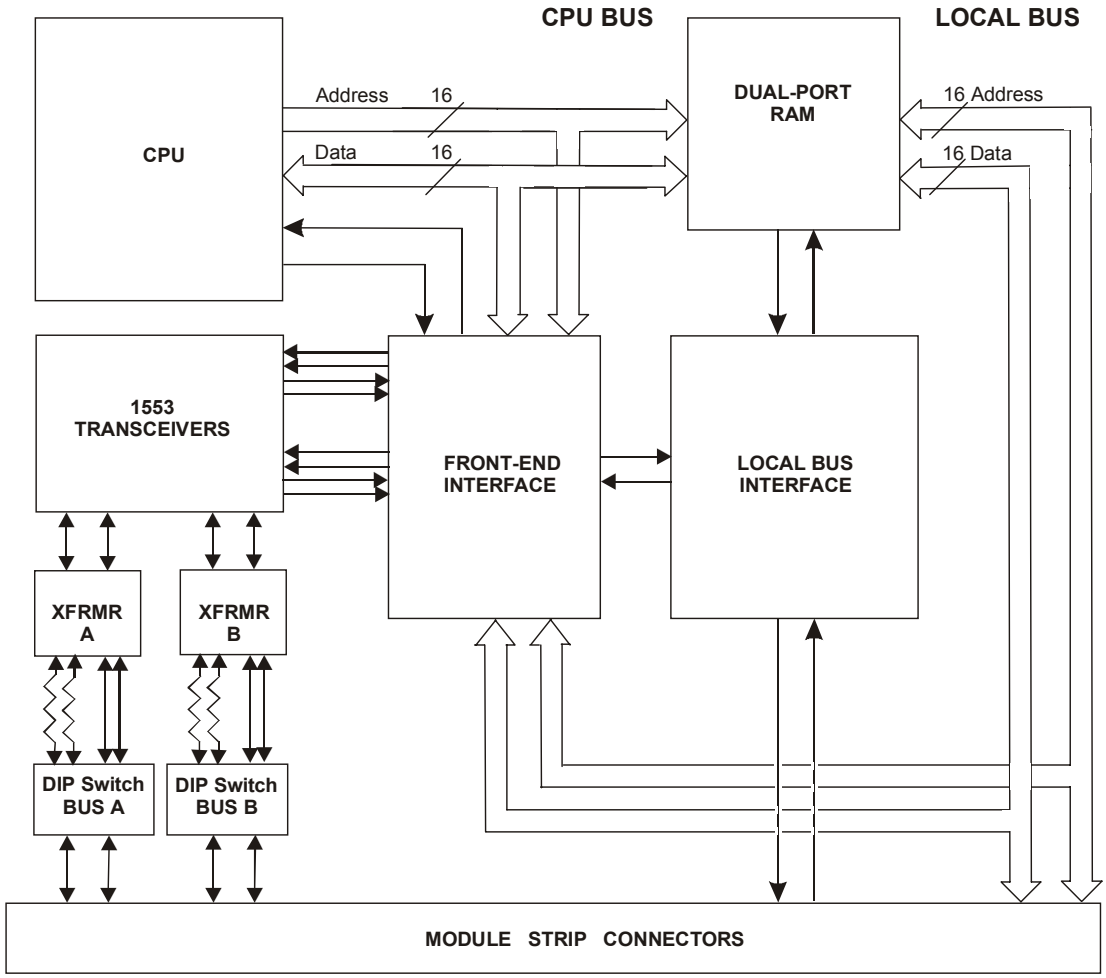

Figure 1-1 *M4K1553Px* Block Diagram

1.1.2 MIL-STD-1760 Considerations

1760 Option only

MIL-STD-1760 implements an enhanced MIL-STD-1553 digital interface for the transfer of digital messages to the remote terminal. The enhancements include additional error detection in the form of checksum. Checksum is mandated on critical control messages and provisional on the remainder of the messages. Implementing this level of error detection ensures a higher degree of error free data integrity requirements than only odd parity provides.

The 1760 option implements checksum error detection capabilities. Checksums are computed as each Data Word is sent or received. If the checksum flag is set on an outgoing message, the checksum will be sent in place of the last Data Word. On an incoming message, the computed checksum is checked against the last Data Word received. If it does not match, the Checksum Error bit is set in the Message Status word.

The1760 option has the additional feature of checksum error injection in BC mode. The user can set the checksum to intentionally send an error, giving the additional capability to test for checksum errors on the receiving RTs.

To order the *M4K1553Px* with the 1760 options, see Chapter 8: **Ordering Information**.

1.2 Installation

To install the *M4K1553Px* module, add the appropriate software for your operating system and then install and configure the hardware.

1.2.1 Software Installation

The standard software included with the *M4K1553Px* module is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com

For information about installing the accompanying software drivers, see the **ReadMe.txt** file on the *M4K1553Px Software Tools* CD or diskettes that came with your module.

1.2.2 Module Installation

Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur module.

1. If the module is supplied separately from the carrier board, *very carefully*, insert the module on the carrier EXC-4000 board. The pin #1 marker (marked with a white rectangle) on the module must be aligned with the white rectangles on the carrier board.
2. 1553 devices may be connected via the I/O connector on the carrier board to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer coupled). Use DIP switches SW1 and SW2 to set the coupling mode to the 1553 bus(es). **7.3 Module Coupling Mode Select DIP switches** on page 7-2.
3. With the computer power source switched **off**, insert the EXC-4000 carrier board with the *M4K1553Px* module into a slot in the computer.
4. Attach the 1553 adapter cable to the carrier board I/O connector and to the bus. **This is very important**: The cables may be connected to or disconnected from the board while power to the computer is turned on but not while the board is transmitting over the bus.

1.3 1553 Bus Connections

For short distances, the *M4K1553Px* may be coupled directly to another 1553 device. To ensure data integrity, make certain that the cable connecting the two devices is properly terminated with 78-Ohm resistors (see Figure 1-2 **Direct Coupled Connection (One bus shown)**).

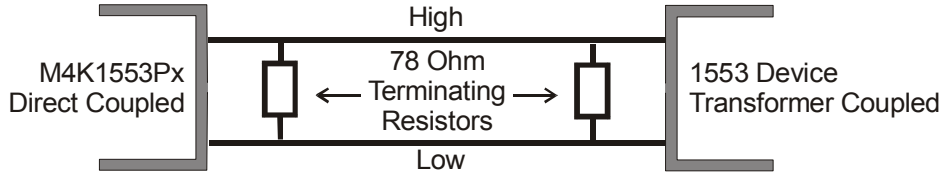

Figure 1-2 Direct Coupled Connection (One bus shown)

If operating in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems. Two terminators are required for each coupler, which services a single bus, i.e. BUS A (see Figure 1-3 **Transformer Coupled Connection (One Bus Shown)**). For more information see our website: www.mil-1553.com.

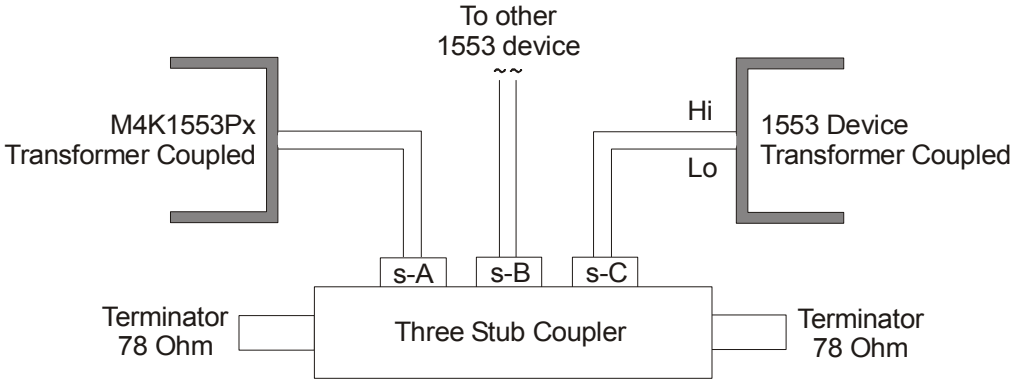

Figure 1-3 Transformer Coupled Connection (One Bus Shown)

Example of MIL-STD 1553 Bus Connection

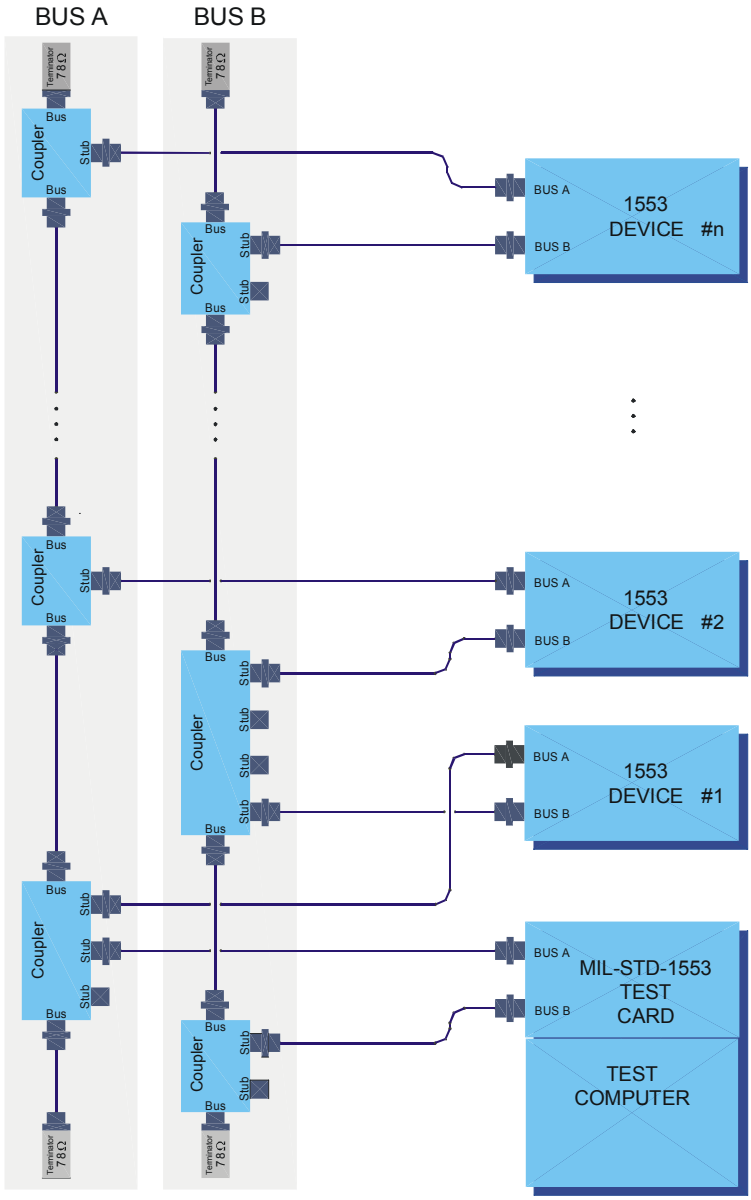

Figure 1-4 MIL-STD 1553 Bus Connection

1.4 *M4K1553Px* General Memory Map

The *M4K1553Px* occupies 64K bytes of the module's 128K-memory space. These 64K bytes are shared between the Control Registers and the Data Block.

Additional Memory	7100 – FFFF H
Reserved	700C – 70FF H
Time Tag Counter	7008 – 700B H
Time Tag Reset Register	7007 H
Reserved	7004 – 7006 H
Options Select Register	7003 H
Reserved	7001 – 7002 H
Software Reset Register	7000 H
Reserved	4800 – 6FFF H
RT Mode BC/Concurrent-RT Mode BM Mode Memory and Control Registers (18K × 8)	0000 – 47FF H Module Base Address

Figure 1-5 *M4K1553Px* General Memory Map

Chapters 2 to 4 of the *User's Manual* explain the operation of the *M4K1553Px* module in each of the three modes: Remote Terminal, BC/Concurrent RT and Bus Monitor. In each chapter the mode specific Memory Map and Control Registers are described.

2 Remote Terminal Operation

Chapter 2 describes *M4K1553Px* operation in Remote Terminal (RT) mode. The following topics are covered:

2.1 RT Memory Map 2-3
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2.11 Error Injection Feature 2-12
2.12 1760 Header Word 2-14
2.13 Program Example: RT Mode 2-14
2.14 Control Register Definitions 2-15

The *M4K1553Px* can be configured to simulate up to 32 remote terminals. The user selects which terminal or terminals are active and can inject errors into message responses.

After receiving the Start command, the module handles the transfer of all messages (see section **2.14 Control Register Definitions**, on page 2-15). Data associated with a particular RT subaddress combination is transferred via a 2K × 8 Look-up Table, which points to one of 200 data blocks. The user loads Data Blocks associated with transmit commands with 1553 data to transmit, and reads received 1553 data from Data Blocks associated with receive commands.

The module will respond properly to messages received with an intermessage gap time of 4 μsec.

The user can choose whether the remote terminal should transmit its 1553 Status Word at the end of a message, even if the message contains *invalid* Data Words (invalid as specified by MIL-STD-1553). Use the **Status Response Register**, on page 2-21, to activate or disable this feature.

The remote terminal transmits its 1553 status word in approximately 4 μsec. Use the RT Response Time register to increase the time it takes the remote terminal to transmit the 1553 status word.

Since most 1553 parameters, such as response time, status word content, etc. are user programmable, the module can operate in various 1553 environments. The module also allows you to enable or disable the 1553 Broadcast function. If broadcasting is enabled, RT address 31 (11111) is reserved; if broadcasting is disabled, all 32 RT addresses are available. See section **2.10 Broadcast Mode**, on page 2-12.

The 1553 Mode Code subaddress identifier can be programmed (see **Mode Code Control Register**, on page 2-24) so that either 31, 0, or both are used to indicate that the 1553 command word is a Mode code.

To determine whether the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID register (test for value = 45 H).
2. Check the Module Status register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values, as written above. For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a '1' to the Start register is referred to as "issuing a Start command."

2.1 RT Memory Map

Figure 2-1 **RT Memory Map** illustrates the RT memory usage.

Additional Memory Area	9000 – FFFF H	1760 Header Exist Table[1]	3EC0 – 3EFF H
RTid Control Table	8000 – 8FFF H	Reserved	3E96–3EBF H
Additional Memory Area	7100 – 7FFF H	Double Buffering RTid Register	3E94 – 3E95 H
Reserved	700C – 70FF H	Double Buffering Bad Block Number Register	3E92 – 3E93 H
Time Tag Counter Word 1	700A – 700B H	Reserved	3E8A – 3E91 H
Time Tag Counter Word 0	7008 – 7009 H	Clear Time Tag on Sync Register	3E88–3E89 H
Time Tag Reset Register	7007 H	Reserved	3E86 – 3E87 H
Reserved	7004 – 7006 H	Module Options Register	3E84 – 3E85 H
Options Select Register	7003 H	Reserved	3E81 – 3E83 H
Reserved	7001– 7002 H	Firmware Revision Register	3E80 H
Software Reset Register	7000 H	Reserved	34C0 – 3E7F H
Data Block Look-Up Table	4000 – 47FF H	1553 RT Vector Words (64 Bytes)	3480 – 34BF H
Module Configuration Register	3FFF H	1553 RT Bit Words (64 Bytes)	3440 – 347F H
Module ID Register	3FFE H	RT Last Command Words (64 Bytes)	3400 343F H
Module Status Register	3FFD H	Reserved	33FD – 33FF H
Start Register	3FFC H	Interrupt Condition Register	33FC H
Message Status Register	3FFB H	Message Stack (42 Blocks)	3300 – 33FB H
Reserved	3FF8– 3FFA H	Word Count Error Table (32 Bytes)	32E0 – 32FF H
Time Tag Resolution Register	3FF7 H	Reserved	3267 – 32DF H
Reserved	3FF5 – 3FF6 H	Mode Code Control	3266 H
RT Response Time Register	3FF4 H	Checksum Blocks Register[1]	3264–3265 H
Error Injection Register	3FF3 H	Reserved	3260 – 3263 H
Reserved	3FF2 H	1553 RT Status Words (64 Bytes)	3220 – 325F H
Message Stack Pointer	3FF0 – 3FF1 H	Active RT Table (32 Bytes)	3200 – 321F H
Status Response Register	3FEF H	1553 Data Blocks (200 Blocks)	0000 – 31FF H
Reserved	3F40 – 3FEE H		
1760 Header Value Table[1]	3F00–3F3F H		

Figure 2-1 RT Memory Map

1. 1760 Options only

2.2 Data Block Look-up Table

Address: 4000–47FF (H)

The received command word's RT Address, T/R Bit, and Subaddress fields are used to index the entries in the (user-programmed) look-up table. Each entry in the table represents a data block number (from 0 to 199 decimal). Each block can contain up to 32 1553 Data Words (64 bytes). Data Block 0 begins at address 0000. Data Block 1 begins at address 0040 (H), etc.

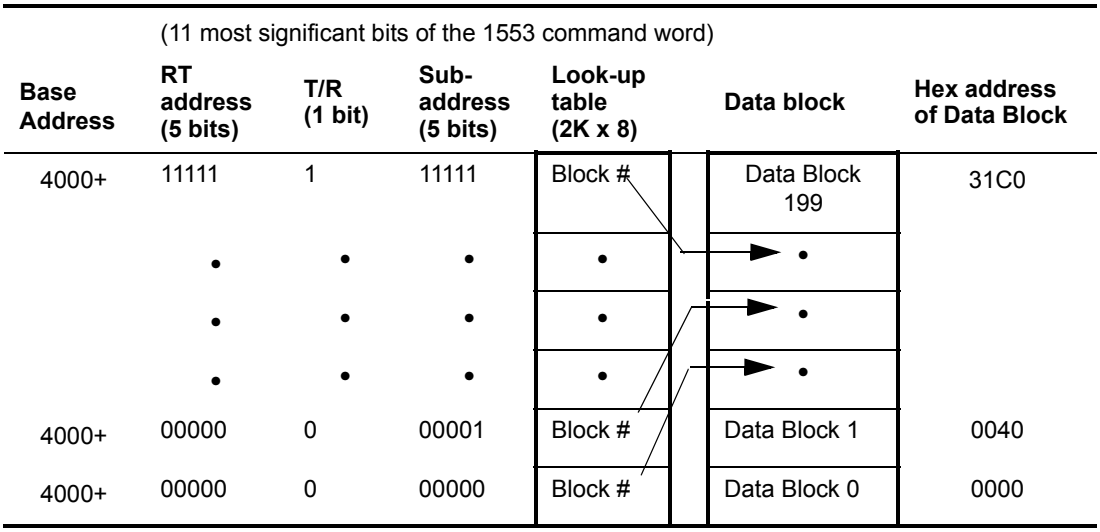

(11 most significant bits of the 1553 command word)
Base Address
RT address (5 bits)
T/R (1 bit)
Sub-address (5 bits)
Look-up table (2K x 8)
Data block
Hex address of Data Block
4000+ 11111 1 11111 Block # Data Block 199 31C0
4000+ 00000 0 00001 Block # Data Block 1 0040
4000+ 00000 0 00000 Block # Data Block 0 0000

Figure 2-2 Data Block Look-up Table

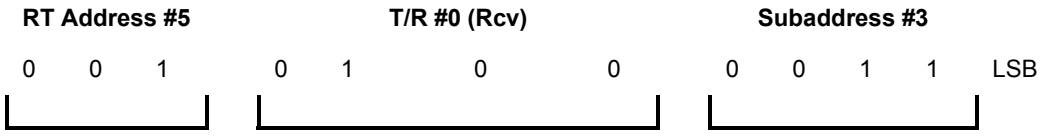
Note:

1. Data Block 0 represents a default for all unassigned RTid's and is not recommended for use by anyone interested in using the data. If the RT does not assign a Data Block to an RTid, the default Data Block is used for both receive and transmit messages.
2. For RT-to-RT messages, when the module is simulating both RTs in an RT-to-RT message transfer, the simulated receiving RT's Data block is not updated with the transmit data. (The data is transmitted over the 1553 bus.)

To create the address to the table

1. Isolate the eleven most significant bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a data block for a 1553 receive message to RT#5, Subaddress 3.



Hex representation = 143 (H)

2. Add the Hex value of this part of the Command Word to the base address of the Look-up table (4000 H).

4000	(H)
+143	(H)
4143	(H)

3. Write the data block number to this location.

Example: `POKE &H4143,01` allocates block #1 for the data of this message. Read the 1553 data out by reading block #1, which starts at address 0040 (H). Each data block, beginning at address 0000 is 64 bytes long (for up to 32 1553 Data Words). The address of a block is obtained by multiplying its block number by 64 (40 H).

2.2.1 Data Storage

The Data Words must be stored and/or read in the following format in the data block:

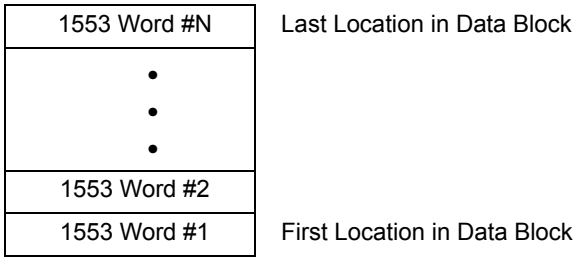


Figure 2-3 Data Storage Sequence

2.3 Active RT Table

Address: 3200–321F (H)

The 32 locations (bytes) of the Active RT table contain the list of active remote terminals. To select an RT to be simulated, set bit 00 in the Active Remote Terminal byte to logic 1. The first active RT byte relates to RT #0, the next to RT #1, and the last location relates to RT #31.

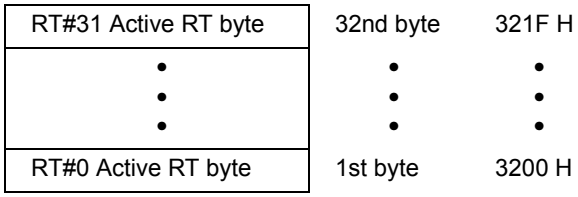


Figure 2-4 Active RT Table: RT Mode

Bit	Bit Name	Description
04-07	**0**	
03	**Inactive Bus B**	1 = Bus B Inactive 0 = Bus B Active If bit 00 is set to 1 and bit 03 is set to 0, the module will respond to all messages received over bus B for this RT; and the module will generate interrupts, if requested to do so. If bit 03 is set to 1, all messages over bus B for this RT will be ignored, regardless of the settings of other bits in this register.
02	**Inactive Bus A**	1 = Bus A Inactive 0 = Bus A Active If bit 00 is set to 1 and bit 02 is set to 0, the module will respond to all messages received over bus A for this RT; and the module will generate interrupts, if requested to do so. If bit 02 is set to 1, all messages over bus A for this RT will be ignored, regardless of the settings of other bits in this register.
01	**Interrupt**	1 = Interrupt 0 = No Interrupt If bit 01 is set to 1, the RT is active and the Interrupt Condition register is enabled, then this module will generate an interrupt as per the **Interrupt Condition Register**, on page 2-24.
00	**Active**	1 = Active 0 = Inactive If bit 00 is set to 0, the RT is not active. If it is set to 1, bits 01, 02, and 03 are checked.

Active RT Byte Definition: RT Mode

2.4 1553 RT Status Words

Address: 3220–325F (H)

These locations are reserved for the 32 1553 RT Status words. Load the desired Status words into their respective locations in the block. The first word relates to RT#0, the next word to RT#1, while the last word relates to RT#31.

For each RT that is to be simulated, all 16 bits of that RT must be defined in its Status word.

In a non-1553B environment (see **Status Response Register**, on page 2-21) the user-defined Status word is sent whenever the RT has to respond with a Status word.

In a 1553B environment (see **Status Response Register**, on page 2-21), the same Status word is sent with the following conditions:

Message Error (Bit 10)	In case an error occurred in the previous message, the Status Word will be sent with the Message Error bit set to 1 if the current message is of type Send Status or Send Last Command. This will occur even if you set the Message Error bit to 0. If you set the Message Error bit to 1, it will always be sent set to 1.
Service Request (SRQ) (Bit 08)	The SRQ bit is set for a RT in the 1553 RT Status Word. Setting the SRQ bit indicates to the BC that the RT/Subaddress requires servicing. The BC with **1760 options** provides the following service: The module will sent out a Mode Code 16 (transmit Vector Word) to get the Vector Word from the RT which contains more information about what needs service. The BC will than send out a transmit message to the Subaddress (provided that it is *not* set to 0) identified in the Vector Word. See section **2.8 1553 RT Vector Words**, on page 2-11.
Busy (Bit 03)	The Busy bit is always sent as you defined it. In the case of Transmit commands, when Busy is set to 1, no Data Words will be transmitted by the RT following the transmission of the status word.

The MIL-STD-1553B Format for the Status word is:

Bit	Bit Name
11–15	RT Address
10	Message Error
09	Instrumentation
08	Service Request
05-07	Reserved
04	Broadcast
03	Busy
02	Subsystem Flag
01	Dynamic Bus
00	Terminal Flag

1553B Status Word

2.5 Message Stack

The module generates a message stack in the dual-port memory. This stack contains information used for post-processing of RT messages. The stack is divided into 42 blocks, each containing three words. The stack operates as a circular buffer. The Message Stack Pointer points to the beginning of the (next) unused block. Only active RT messages are stored, **Figure 2-5** illustrates one block.

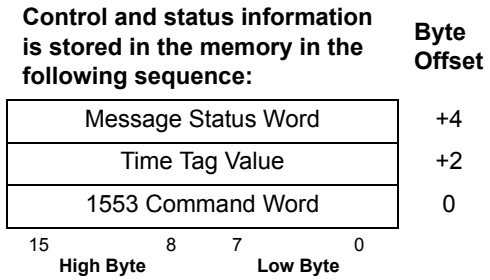


Figure 2-5 Message Stack Block Structure

How the module updates an RT-to-RT message

When an RT-to-RT message is received, where the module is functioning as both RTs, the Message stack is updated as follows:

Two message stack blocks are utilized.

1. The 1553 Receive command word is written into the *first* message stack block.
2. The RT-to-RT bits in *both* Message Status Words are set to 1.
3. The module updates the Time Tag word in the *second* stack block and the *second* Message Status Word. The module updates only the RT-to-RT bit in the *first* Message Status Word to Active status.
4. The 1553 Transmit command word is written into the *second* stack block.

2.5.1 Message Status Word

The Message Status word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the 1553 Status word (see **1553 RT Status Words**, on page 2-7). The contents of the Message Status word are described below.

Note:

1. A logic 1 indicates the occurrence of a status flag
2. The Message Status Word is valid only when bit 15, End of Message, is turned on.

Bit	Bit Name	Description
15	End Of Message	Message transfer completed
14	Bus A / B	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
13	Checksum Error	The computed checksum (on an incoming message) does not match when checked against the last Data Word received. See section **1.1.2 MIL-STD-1760 Considerations**, on page 1-3
11-12	Reserved	Set to 0
10	Tx Time Out	Module, acting as receiver in RT-to-RT message, did not sense a transmitter status word (in 14 μsec.)
09	Reserved	Set to 0
08	1760 Header Error	Header Word Received does not match the value set in the Header Value table. See section **1.1.2 MIL-STD-1760 Considerations**, on page 1-3
07	Invalid Word Received	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity)
06	Reserved	Set to 0
05	Word Count Error (Receive Message)	Incorrect number of words received in the message
04	Broadcast Message	Broadcast Command Word received
03	Incorrect Sync Received	Sync of either the Command or the Data Word(s) is incorrect
02	Non- Contiguous Data (Receive Message)	Invalid gap between received 1553 words
01	RT-RT Message	RT-to-RT message received where module was simulating both RTs
00	Error	Error occurred (The error type is defined in one of the other message status bit locations.)

Message Status Word

2.5.2 Time Tag

Read only

The Time Tag value is a 16-bit word that can be used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag uses a 32-bit, free-running counter whose resolution is set by the Time Tag Resolution register. This register has a resolution of 4 µsec. per bit. The equation to determine the Time Tag resolution = (register value + 1) × 4 µsec.

Note: Only the lower 16 bits of the counter are written to dual-port RAM.

Example:

Register value = 0 → Counter's resolution = 4 µsec

Register value = 4 → Counter's resolution = 20 µsec

To reset the Time Tag counter (to 0) any time, write to the **Time Tag Reset Register,** on page 2-17.

When the first command of each message is received, the value of the 16 lower bits of the Time Tag Counter register are written to dual-port RAM.

Note:

1. Only the lower 16 bits of the counter are written to the dual-port RAM
2. The counter's value can be read at any time by reading the Time Tag Counter addresses (see page 2-17).
3. The counter can also be clocked and/or reset from an external source (see section **7.4 Connectors**, on page 7-3).

Example: How To Calculate Elapsed Time

Time Tag Resolution register = 03 (initialized before Start command)

Time Tag values (read during or after message transfers):

Low = 0040 (H)
High = 0010 (H)

Time elapsed since Start command

= (Time Tag register value) × (Time Tag Resolution value + 1) × (4 msec)

= 100040 (H) × (03 + 1) × 4 msec

= 1048640(Dec) × (4 × 4 µsec) = 16778240 µsec (16778.24 msec. = 16.778 sec.)

2.5.3 1553 Command Word

The Command word location contains the 1553 Command word associated with the message.

Only active RT Command words are stored.

2.5.4 RT-to-RT Messages

When the module is operating as both RTs in an RT-to-RT transfer:

- The module transmits both 1553 Status and Data Words onto the bus.
- The module does *not* copy the Transmit data block into the Receiver data block area (pointed to by the Look-up Table pointer).

2.6 RT Last Command Words

Address: 3400–343F (H)

The Last Command Word locations are reserved for the 32 1553 Last Command words. The module writes to these locations at the end of each message transfer (for active RTs only). The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used for the implementation of the Transmit Last Command Word Mode code.

Note: Only Command words of valid messages containing no errors are recorded in this table.

2.7 1553 RT BIT Words

Address: 3440–347F (H)

The RT BIT word locations are reserved for the 32 1553 BIT words. Load the desired BIT words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used to implement the Transmit BIT Word Mode code.

2.8 1553 RT Vector Words

Address: 3480–34BF (H)

The RT Vector Word locations are reserved for the 32 1553 Vector words. Load the desired Vector words into the corresponding locations in the block. The first word is for RT#0, the next word is for RT#1, and the last word is for RT#31. These words are used to implement the Transmit Vector word Mode code.

Vector Word Setting (bit 15)	Description
1	Indicates that the contents of the Vector Word are user-defined. The module will do nothing.
0	The BC will build a transmit message (RT-to-BC) to this RT, with the Subaddress and Word Count as indicated in the corresponding bit positions of the Vector Word. If the Vector Word Subaddress field is set to 0 (or if the whole Vector Word is set to 0) this is as if requesting the module to send a mode code of 0 as an RT-to-BC command. This does not make any sense, and therefore, the module disregards this request.

Vector Word Bit

2.9 Mode Codes

The user can program the Subaddress code that will indicate that a Mode command has been received. Either or both of the following codes can be used: 11111 and 00000. The Mode Code Control register must be programmed as described in section **2.14.24 Mode Code Control Register**, on page 2-24.

The module handles all dual-redundant 1553B Mode codes. The Word Count field is decoded according to MIL-STD-1553B. One of the Mode codes (Synchronize with Data Word) is operated upon as a standard message transfer, using the Data Block Look-up table. When the module encounters the Synchronize with Data Word Mode code, the command word's RT Address, T/R bit, and Subaddress fields are used as a pointer to the Look-up table. The table entries that are addressed when the T/R bit = 0 and Subaddress = 00000 or 11111 should contain a Data Block number (0–199) indicating where the Synchronize with Data Word's Data Word should be stored.

The data associated with mode codes (Transmit Last Command, Transmit Bit word, and Transmit Vector word) is set using the dedicated blocks in the on-module memory (described in **RT Last Command Words,** on page 2-11, **1553 RT BIT Words,** on page 2-11, and **1553 RT Vector Words,** on page 2-11).

2.10 Broadcast Mode

To operate the module in the broadcast mode, select the appropriate bit settings as defined in the **Options Select Register**, on page 2-17.

When operating in Broadcast mode, the active RT Look-up table entry must be set for RT#31 as Not Active. The module reads the **Options Select Register**, on page 2-17, to determine whether the module is operating in Broadcast mode.

In Broadcast mode, the module stores the received message in a 1553 data block area in the same way as standard message formats. RT address, T/R bit, and Subaddress are used as a pointer to the Data Block Look-up table memory.

Note: When operating in Broadcast mode, the Broadcast bits in the 1553 Status words are *not* updated by the module's processor.

2.11 Error Injection Feature

The module allows two types of error injection:

- Global (for all RTs)
- Per RT The global errors such as Sync and Non-Contiguous data are described in **Error Injection Register,** on page 2-21. These errors are either ON or OFF for all RTs. The ability to inject a 1553 Word Count error, however, can be set per RT.

2.11.1 Word Count Error Table

Address: 32E0–32FF (H)

The Word Count Error is selected by writing to the Word Count Error table, which contains 32 bytes (one per Remote Terminal). The first byte is for RT#0, the second toRT #1, and the last byte is for RT#31. The contents of each location, controls the number of 1553 words (±3 words) in the message. The variation is an offset, relative to the 1553 Command word's Word Count field. The resulting message (if an error is programmed) must contain at least one Data Word.

Upon power-up and software reset, the module sets the Word Count Error Table to the default value, 00.

The user must set the Word Count Error register before issuing a Start command to the module. To modify the Word Count Error register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register**, on page 2-19).

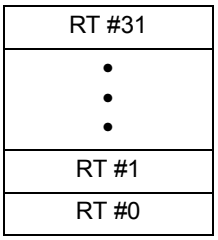


Figure 2-6 Word Count Error Table Address

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word Count Error Byte Values

2.12 1760 Header Word

1760 Options only

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The header word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first Data Word of the message.

The 1760 option provides predefined values, and these are preset on the *M4K1553Px* module.

For descriptions of the **1760 Header Value Table** and **1760 Header Exist Table**, see page 2-22.

2.13 Program Example: RT Mode

All values are in Hex unless otherwise states

BASIC Instruction	Remarks
`10 POKE &H3FFF,02`	Set the Configuration register to RT mode.
`20 POKE &H3FF2,xx`	Set the Variable Amplitude register.
`30 POKE &H3201,1`	Enable RT #1.
`40 POKE &H3204,1`	Enable RT #4.
`50 POKE &H3222,00`	Set the Status word of RT #1 to 0800.
`60 POKE &H3223,08`	
`70 POKE &H3228,00`	Set the Status word of RT #4 to 2000.
`80 POKE &H3229,&H20`	
`90 POKE &H3FF7,xx`	Set the Time Tag Resolution register.
`100 POKE &H3266,00`	Set the Mode Code Control register to Subaddress 0 & 31.
`110 POKE &H3FF3,00`	Set No global error injection.
`120 POKE &H4xxx,1`	Load block number 1 for data storage into Look-up table xxx.
`130 POKE &H4yyy,2`	Load block number 2 for data storage into Look-up table yyy.
`140 POKE &H3FFC,1`	Set the Start register to 1 to start RT mode.
`150 STOP`	

Program Example – RT mode

2.14 Control Register Definitions

RT Identifier (RTid)

The RTid is referred to frequently in the RT control registers. The RTid is defined as an RT address, T/R bit value and RT subaddress combination. The structure of the RTid is illustrated below:

5 bits	1 bit	5 bits
RT ADDRESS	T/R	SUBADDRESS

RT Identifier

Example: RT#5, Transmit, Subaddress 6 would be represented as 00101 1 00110 or 0×166. This value can be isolated from a Command Word by shifting the Command Word 5 bits to the right.

See **To create the address to the table**, on page 2-4.

2.14.1 RTid Control Table

Address: 8000–8FFF (H)

The RTid Control Table is a block of memory, one word per RTid, to store settings for a number of features. For the features to be implemented the following conditions must be met:

1. The RT is active
2. The Message is for this specific RTid
3. The bit must be set

Bit	Bit Name	Description
06–15	Reserved	
05	Double buffer datablock usage flag	The bit indicates which block of the double buffering pair to use for storing the data for this RTid. 0 = [**Default**] The module detects a receive message. The module stores the data at the even-numbered block number indicated in the Look-up table. When the module completes writing all the Data Words to the block, the module sets this bit to 1. This indicates to write to the odd-numbered block the next time receive data comes in for this RTid. 1 = The module detects a receive message. The module stores the data at the odd-numbered block, whose number is one more than the even-number indicated in the Look-up table. When the module completes writing all the Data Words to the block, the module sets this bit to 0. This indicates to write to the even-numbered block the next time receive data comes in for this RTid.

RTid Control Table

04	Double Buffering (Receive) selected	The bit indicates that the module will double buffer data for the receive messages for this RTid. When the module receives messages for an RTid, the data is stored in the assigned datablock. If no datablock is assigned, data is stored in the default datablock (number 0). When two messages arrive for the same RTid, the data of the second message will overwrite the data of the first message. To preserve the data of the first message long enough to be able to read it before it gets overwritten, use a double buffering scheme to save the data of the last two messages; i.e., use two buffers, alternatively, so that the module can capture data to one buffer, and simultaneously the user can read data from the other buffer. To implement double buffering, the module requires that the datablock assigned to this RTid be an even number. The module then reserves the following odd-numbered block as the paired block for use in double buffering. **Note:** If Double Buffering is enabled for this RTid, and the block number selected is odd, do *not* do double buffering. Set: 1. A flag at bit 02 in the **Message Status Register** [3FFB H]; 2. Write the selected (odd) block number to the **Double Buffering Bad Block Number Register** [3E92 H] to indicate the error; 3. Write to RTid to the **Double Buffering RTid Register** [3E94 H].
03	Inactive	The RTid is inactive – do not process the message at all; the RT does not send back a Status Word. **Note:** RT response time must be set to at least 5 msec., otherwise there will be extraneous words on the bus.
02	Illegalization	The RT does not want to respond to this RTid. Set the Message Error (ME) bit in the RT Status Word (STW) [bit 10]. For **BC-to-RT** (receive) messages — continue processing as per regular algorithm, and write the ME bit in the STW. For **RT-to-BC** (transmit) messages — do not send any data or STW. For **RT-to-RT** messages — receive part: write the ME bit in the STW; transmit part: do not send any data or STW.
01	Interrupt on Error	Generates an interrupt on error
00	Interrupt on end of message	Generates an interrupt on end of message

RTid Control Table (cont.)

2.14.2 Time Tag Counter

Address: 7008–700B (H)

Read only

The user may read the current free-running, 32-bit Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

The counter is reset upon power-up or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting.

The counter must be read in the following sequence:

1. Read 7008 H (16 bit, read only)
2. Read 700A H (16 bit, read only)

7008 H contains the Lo word; 700A H contains the Hi word. The Time Tag resolution register sets the resolution of the counter (See **Time Tag Resolution Register**, on page 2-20)

2.14.3 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset register to reset the module's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

Note: The counter is also reset from an external source. See section **7.4.2 Connector Pin Assignments: Px Configuration**, on page 7-4.

2.14.4 Options Select Register

Address: 7003 (H)

Write Only

Write to the Options Select register to select whether RT address 11111 (RT #31) is interpreted as a valid RT address or as a Broadcast address.

Bit	Description	
02–07	Don't Care	
01	Reserved	
00	1	Broadcast option is active. RT#31 is Broadcast Address. No RT Status Word will be transmitted.
	0	Broadcast option is inactive, RT#31 is a regular RT.

Options Select Register

Note: The Options Select register is reset at power-up (all bits set to 0). This register is not affected by a software rest and can be modified at any time without having to start and stop module operation.

2.14.5 Software Reset Register

Address: 7000 (H)

Set the Software Reset register to reset the module (data field = don't care)

Bit	Description
00–07	Don't Care

Software Reset Register

Note: Software Reset erases all locations in the dual-port RAM, module status, module ID and Firmware registers are written by the module after the reset operation is completed.

2.14.6 Module Configuration Register

Address: 3FFF (H)

Use the Module configuration register to set the operating mode of the module.

Set the Module Configuration register before issuing a Start command to the module. To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command (see **Start Register**, on page 2-19).

Hex Value	Operating Mode
02	RT Mode

Module Configuration Register

2.14.7 Module ID Register

Address: 3FFE (H)

The Module ID register contains a fixed value that can be read by the initialization routine to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

2.14.8 Module Status Register

Address: 3FFD (H)

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to '1'.

Bit	Description
07	1 = Module type is M4K1553Px
05–06	X 'Don't Care'
04	1 = Module Halted 0 = Module Running
03	1 = Self-test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 - Module ready

Module Status Register

Note: Module operation stops after the Start bit in the Start Register is cleared. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic '1'.

2.14.9 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the module. The user can Start or Stop the RT operation, modify RT parameters (example: the Error Injection register or Response Time), and then issue a new Start command in real time.

For more information about Bit 04 (Module Halted/Running) in the Module Status Register, see the note in Module Status Register.

Bit	Description
01–07	0
00	1 = Start Operation 0 = Stop

Start Register

Note: The user can start concurrently by sending a low TTL pulse of 100 nsec. Minimum to the EXSTARTn pin, see section **7.4.2 Connector Pin Assignments: Px Configuration**, on page 7-4.

2.14.10 Message Status Register

Address: 3FFB (H)

The Message Status register indicates that a 1553 message has been received. A logic '1' indicates active condition. This bit is also set for messages with errors.

Bit	Description
01–07	0
00	Message Content

Message Status Register

Note: After reading, reset the Message Complete bit; the module does not reset this bit.

2.14.11 Time Tag Resolution Register

Address: 3FF7 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 µsec.

To determine the Time Tag Counter's Resolution, use the following equation:

= (Time Tag Resolution register value + 1) × 4 µsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the module. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-19).

2.14.12 RT Response Time Register

Address: 3FF4 (H)

The RT Response Time register sets the Response Time of the Remote Terminal. The resolution of the Response Time register is 155 nsec. per bit. The minimum time is approximately 4 µsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 µsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 µsec.

The Response Time register must be set before issuing a Start command to the module. To modify the Response Time register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-19).

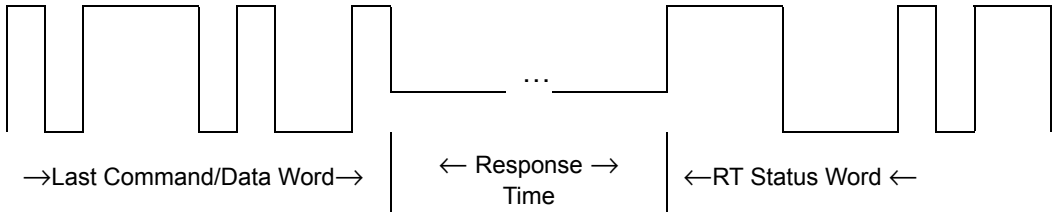


Figure 2-7 RT Response Time Definition

Example: To request a Response time of 9 µsec:
Write 32 to the RT Response Time Register
$32 \times 0.155 \cong 5$ µsec + 4 µsec = 9 µsec

2.14.13 Error Injection Register

Address: 3FF3 (H)

The Error Injection register is a global register that allows the user to select the type of error to be injected in a transmitted message. When the module receives a Start command (issued by writing to the Start register), the module reads this register.

To modify the Error Injection register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-19).

Bit	Description
07	Data Word Sync Error (Data Words Sent With Command Sync)
06	Reserved (Set to 0)
05	Status Word Synchronization Error (Status Word Sent With Data Sync)
03–04	Reserved (set to 0)
02	Non-Contiguous Data (Between First and Second Data Word)
00–01	Reserved (set to 0)

Error Injection Register

2.14.14 Message Stack Pointer

Address: 3FF0–3FF1 (H)

The Message Stack pointer indicates the Message Stack position. After the entire message is received, the Message Stack pointer is updates (incremented by 6). This word id initialized to 3300 (H) and circulates in the Message Stack between 3300 (H) and 33F6 (H).

2.14.15 Status Response Register

Address: 3FEF (H)

The Status Response register is used to control the Status Response mode of operation.

After a Receive message, you can respond with a 1553 Status word even if an invalid 1553 Data Word was received. The user can also select a 1553 environment, which will affect some 1553 RT Status word bits. (See **1553 RT Status Words,** on page 2-7).

The Status Response register must be set before issuing a Start command to the module. To modify the Status Response register, issue a Stop command, modify the register, then, issue a Start command. (See **Start Register,** on page 2-19).

Bit	Description	
02–07	0	
01	Environment:	0 = 1553B 1 = non-1553B
00	On Error	0 = Suppress Status 1 = Send Status

Status Response Register

2.14.16 1760 Header Value Table

Address: 3F00–3F3F (H)

1760 Options only

Write to the 1760 Header Value table to set the value you expect to receive in the first Data Word of the BC-to-RT or RT-to-RT message. The 1760 option provides predefined values, and these are preset on the *M4K1553Px* module.The user can change the preset values.

Address	Hex Value	Associated Subaddress
3F16 H	0400	11
3F1C H	0422	14

Receive Subaddress: RT Mode

2.14.17 1760 Header Exist Table

Address: 3EC0–3EFF (H)

1760 Options only

The 1760 Header Exist Table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether the module should expect a header word for BC-to-RT or RT-to-RT messages directed to that subaddress.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on the M4K1553P*x* module.

To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value Table.

Bit	Description	
01–15	Reserved	
00	1	Module should expect a Header word
	0	Module should **not** expect a Header Word

1760 Header Exist Table

Address	Hex Value	Associated Subaddress
3ED6 H	0001	11
3EDC H	0001	14

Receive Subaddress: RT Mode

2.14.18 Double Buffering RTid Register

Address: 3E94–3E95 (H)

The Double Buffering RTid Register indicates the associated RTid for which the user attempted to set an erroneous odd-numbered block.

2.14.19 Double Buffering Bad Block Number Register

Address: 3E92–3E93 (H)

The Double Buffering Bad Block Number Register indicates the erroneous, odd-numbered block selected for use in double buffering.

2.14.20 Clear Time Tag on Sync Register

Address: 3E88–3E89 (H)

Set the lower byte [3E88 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag Registers [7008–700B H] (resets to 0) upon receipt of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Set the higher byte [3E89 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag Registers [7008–700B H] (resets to 0) upon receipt of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

2.14.21 Module Options Register

Address: 3E84–3E85 (H)

Read only

The Module Options register is a 16-bit register that identifies the type of on-module firmware.

Bit	Description	
15	Reserved	
14	'1' M4KPx	
10–13	Reserved	
09	'1' 1760	
08	'1' 1553	
00–07	Module Type:	4D H = PMx module 50 H = Px module

Module Options Register

2.14.22 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-module firmware. The value 0001 0010 would read as revision level '1.2'.

2.14.23 Interrupt Condition Register

Address: 33FC (H)

The Interrupt Condition register allows the user to enable an interrupt trigger. The bits work in conjunction with the Interrupt bit in the Active RT table. When a message is received by an RT for which the Active RT interrupt bit is set, the module will check the Interrupt Condition register.

If the module has completed receiving the Command Word and the Begin Data bit is also set, an interrupt trigger will be generated.

If the module has completed processing the message and the Message Complete bit is also set, an interrupt trigger will be generated.

Set the Interrupt Condition register before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-19)

Bit	Description
02–-07	0
01	1 = Message Complete
00	1 = Begin Data

Interrupt Condition Register

2.14.24 Mode Code Control Register

Address: 3266 (H)

The Mode Code Control register allows the user to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

Set the Mode Code Control register before issuing a Start command to the module. To modify the Mode Code Control register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** on page 2-19).

Bit	Description		
02–07	0		
00–01	Bit 01	Bit 00	Subaddresses recognized as Mode Code
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

2.14.25 Checksum Blocks Register

Address: 3264–3265 (H)

Write a value to the Checksum Blocks register to set the data blocks for which the module should compute a checksum value. The module will compute a checksum value for those data blocks whose numerical index is less than the value stored in this register. Maximum value is 200.

Example: Write 20 to the Checksum Blocks register when you want data blocks 0–19 to have a checksum value. This causes the module to:

1. Transmit a checksum value as the last word in the data block (transmit message).
2. Check the last word in the data block for a checksum value (receive message).

3 BC/Concurrent-RT Operation

Chapter 3 describes *M4K1553Px* operation in Bus Controller/Concurrent-Remote Terminal mode. The topics included are:

3.1 BC/Concurrent-RT Memory Map 3-2
3.2 Instruction Stack. 3-3
3.3 Remote Terminal Simulation 3-11
3.4 Message Block Formats. 3-12
3.5 Continuous or One-Shot Message Transfers. 3-14
3.6 1760 Header Word. 3-15
3.7 Program Example: BC/Concurrent-RT Modes. . . . 3-16
3.8 Control Register Definitions 3-17

The *M4K1553Px* can simultaneously operate as the Bus Controller and up to 32 Remote Terminals. The messages and the instruction stack are loaded as for BC operation.

In Concurrent-RT mode, load message blocks with the RT's 1553 Status and Data Words for those Remote Terminals that you are actively simulating. These words must be loaded into the appropriate locations in the message blocks in the sequence that the 1553 words appear on the 1553 bus.

Note: The requirement for loading the message blocks only applies to RTs that the user is actively simulating. For RTs that are not active (not simulated by the module), the user can leave the corresponding locations blank in the associated 1553 message blocks.

The Remote Terminals simulated in BC/Concurrent-RT mode have a minimum response time of approximately 4 μsec.

To determine if the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID register (test for value = 45 H).
2. Check the Module Status register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a '1' to the Start register is referred to as issuing a Start command.

3.1 BC/Concurrent-RT Memory Map

Figure 3-1 illustrates the BC/Concurrent-RT Memory usage..

Additional Memory Space	7100–FFFF H		
Reserved	700C–70FF H		
Time Tag Counter Word 1	700A–700B H		
Time Tag Counter Word 0	7008–7009 H		
Time Tag Reset Register	7007 H	Instruction Counter	3FEA–3FEB H
Reserved	7004–7006 H	Minor Frame Time Register (16 bits)	3FE8–3FE9 H
Options Select Register	7003 H	Minor Frame Time Multiplier Register (16 bits)	3FE6–3FE7 H
Reserved	7001–7002 H	Replay Register	3FE5 H
Software Reset Register	7000 H	Reserved	3F80–3FE4 H
Message Block Area[1]	4800–6FFF H	1760 Header Value Table[2]	3F40–3F7F H
Reserved	4000–47FF H	Reserved	3F00–3F3F H
Module Configuration Register	3FFF H	1760 Header Exist Table[2]	3EC0–3EFF H
Module ID Register	3FFE H	Reserved	3E8C–3EBF H
Module Status Register	3FFD H	Send Time Tag on Sync Register	3E8A–3E8B H
Start Register	3FFC H	Clear Time Tag on Sync Register	3E88–3E89 H
Interrupt Condition Register	3FFB H	Reserved	3E86–3E87H
Message Status Register	3FFA H	Module Options Register	3E84–3E85 H
RT Response Time Register	3FF9 H	Reserved	3E81–3E83 H
Reserved	3FF7–3FF8 H	Firmware Revision Register	3E80 H
Loop Count Register	3FF6 H	Reserved	3426–3EF7 H
Bit Count Register	3FF5 H	Asynchronous Start Flag	3424–3425 H
Word Count Register	3FF4 H	Asynchronous Frame Pointer Register (16 bits)	3422–3423 H
BC Response Time Register	3FF3 H	Asynchronous Message Count Register (16 bits)	3420–3421 H
Variable Amplitude Register	3FF2 H	Active RT Table (32 bytes)	3400–341F H
Stack Pointer	3FF0–3FF1 H	Instruction and Message Block Area	0000–33FF H
Frame Time Multiplier Register	3FEE–3FEF H		
Frame Time Resolution Register	3FEC–3FED H		

Figure 3-1 BC/Concurrent-RT Memory Map

1. Internal Concurrent Monitor Option - see **Internal Concurrent Monitor Option,** page 5-1
2. 1760 Options only

3.2 Instruction Stack

The Instruction Stack is used to program the module. The stack is divided into instruction blocks, each containing four words. The block contains control information (that the user writes) and status information (that the module writes). Figure 3-2 **Instruction Block Structure: BC/Concurrent-RT Mode** illustrates one instruction block.

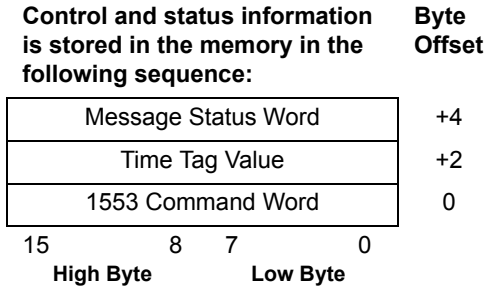


Figure 3-2 Instruction Block Structure: BC/Concurrent-RT Mode

3.2.1 Message Status Word

The Message Status word indicates the status of the message transfer. The module creates this word. Do not confuse this word with the 1553 Status word. (See the section **2.7 1553 RT Status Words,** page 2-7). The contents of the Message Status word are described below.

Note:

1. A logic 1 indicates occurrence of status flag.
2. The Message Status Word is valid only when bit 15, End of Message, is turned on.

Bit	Bit Name	Description
15	**End Of Message**	Message transfer completed
14	**Checksum Error**	The computed checksum (on an incoming message does not match when checked against the last Data Word received. [1760 Option only] See section **1.1.2 MIL-STD-1760 Considerations** on page 1-3.
13	**Incorrect 1553 Channel**	Remote Terminal response was not received on the active 1553 channel.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit was set in the RT Status word (other than the Message Error bit). The error bit is not set in conjunction with this bit.
10	**Invalid Message Error**	A 1553 message-level error occurred (e.g. Word count, incorrect sync); details in the bits described below.
09	**Response Time Failure**	RT responded late (see BC Response Time Register, page 4-25).
08	**1760 Header Word**	Header Word received does not match the value set in the Header Value Table. [1760 Option only] See section **1.1.2 MIL-STD-1760 Considerations** on page 1-3
07	**Invalid Word Received**	At least one invalid 1553 word received (e.g., bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Lo**	RT transmitted too few words.
04	**Incorrect RT Address**	1553 Status word received did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the status or Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Reserved**	Set to 0
00	**Error**	Error occurred. The error type is defined in one of the other message status bit locations.

Message Status Word

3.2.2 Intermessage Gap Time

The Intermessage Gap Time (IGT) value is a 16-bit word that the user writes, that allows a unique intermessage delay time to be inserted between the current message and the next message. The minimum IGT is approximately 4 μsec. The maximum IGT is approximately 10 msec. that can be extended up to approximately 80 seconds, using the IGT counter value. (See **Intermessage Gap Time Counter**). The value in the word is added to this minimum time. The resolution of this word is 155 nsec. per bit.

3.2.3 Intermessage Gap Time Counter

The Intermessage Gap Time counter (IGT_counter) is a 16-bit word written by the user, allowing to increase the Intermessage Gap Time by repeating the number of times the Intermessage Gap Time value is used (bits 00–12). Use bit 13 in this register to instruct the module to generate an interrupt when this specific message completed. Bits 14 and 15 allow the user to generate a checksum and inject an incorrect value into the checksum (See section **1.1.2 MIL-STD-1760 Considerations** on page 1-3.)

Bit	Bit Name	Description
15	**Chk_Sum_On**	Generates a checksum **[1760 option only]**
14	**Chk_Sum_Err_Inj**	Injects an incorrect value into the checksum **[1760 option only]**
13	**Int_On_Select_Msg**	1 = Generate an interrupt when this specific message is completed. To set general interrupt conditions. See **Interrupt Condition Register,** page 3-20
00-12	**IGT_counter**	Write a value to increase the IGT by repeating the number of times the IGT value is used. For example, if the counter is set to 0, then the gap time is not repeated; and depends on the contents of the IGT location. If the gap time counter is 1, then the gap time is repeated once and equals the IGT value × 2, etc. **Note:** To ensure maximum IGT accuracy when using the IGT_counter, use the largest possible value for the IGT word and the smallest value for the IGT_counter, for a given desired intermessage gap time.

Intermessage Gap Time Counter

3.2.4 Message Block Pointer

The Message Block pointer is a 16-bit word that the user writes to point to the beginning of a 1553 message block.

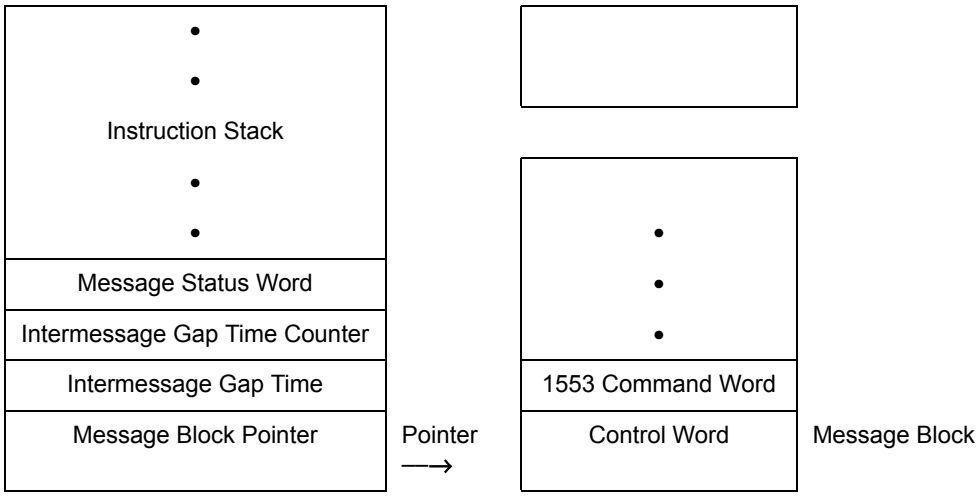


Figure 3-3 Message Block Pointer: BC/Concurrent-RT Mode

3.2.5 Message Block

The message block can be loaded anywhere in the Instruction Stack/Message Block area (See **Figure 3.1 BC/Concurrent-RT Memory Map** on page 3-2). Message blocks do not have to be stored in sequential locations in the memory since the Message Block pointers point to the message blocks in sequence.

Each block contains a 1553 message plus its Control word. This Control word is written into the first word of each block. The Control word instructs the module which type of message to transmit (i.e., RT to RT, Mode code, Broadcast, Error injection, etc.). The size of the message block is variable and depends on the size of the message itself.

The descriptions of the various message block formats (i.e., BC-to-RT, RT-to-BC and RT-to-RT) are illustrated in section **3.4 Message Block Formats** on page 3-12.

For a description of each bit see section **3.2.6 Control Word** on page 3-7.

3.2.6 Control Word

Logic 1 enables the function, 0 disables the function.

Bit	Bit Name	Description
15	**Stop On Error**	Message error stops BC operation. Restart by writing to the Instruction Count register and issue a Start command.
14	**Parity Error**	Selects Even parity in 1553 word.
13	**Halt/Continue**	1 = Halt; stops BC transfer operation. This bit must be reset to 0 to Run or Continue.
12	**Word Count Error**	Transmits fewer or more words than are indicated by the Word Count field (see **Word Count Register** on page 3-23. This function is valid for BC-to-RT messages only.
11	**Bit Count Errors**	Transmits invalid number of bits in 1553 words (see **Bit Count Register** on page 3-22)
10	**Incorrect Sync**	Transmits incorrect sync. Data type Sync is transmitted in the Command word.
09	**Non-Contiguous Data**	Transmits the first 1553 Data Word with invalid Gap Time (between Command and Data Word).
08	**Error Placement/ Error Injection Enable**	For BC-to-RT, Broadcast Receive, and Mode Code with Data messages, bit 08 selects the Parity, Sync, Bit Count error injection placement: 0 in Command word 1 in Data Words For other message types, this bit must be set (=1) to enable error injection.
07	**Bus A/B**	Selects active 1553 bus: logic 1 selects bus A; logic 0 selects bus B.
06	**Auto Bus Switch**	On error, the BC will retry message transfer on alternate bus Auto-retry must be selected
04–-5	**Auto Retry Code**	On error, selects the number of retries before transferring the next message:

Bit 05	**Bit 04**	**Description**
0	0	No Retries
0	1	1 Retry
1	0	2 Retries
1	1	3 Retries

00–03	**Command Code**	**03**	**02**	**01**	**00**	**Description**
		0	0	0	0	Transmit Command (RT to BC)
		0	0	0	1	Receive Command (BC to RT)
		0	0	1	0	RT-to-RT Command
		0	0	1	1	Mode Code
		0	1	0	0	Broadcast Receive Command
		0	1	0	1	Broadcast RT-to-RT Command
		0	1	1	0	Broadcast Mode code
		0	1	1	1	Skip Message [1]
		1	0	0	0	Jump Command [2]
		1	1	1	1	Minor Frame Command [3]

BC/RT Control Word

1. see **3.2.8 Skip Message** on page 3-8
2. see **3.2.9 Jump Command Operation** on page 3-8
3. see **3.2.10 Minor Frame Operation** on page 3-9

3.2.7 Halt Operation

Normally set the Halt Operation bit to logic 0 before writing to the Start register. In real-time (during BC execution), the user sets this bit to logic 1. When operating on that particular message block's Control word, the module will halt transfer operations until the bit is reset to logic 0.

When the module detects that the Halt bit is set, it sets the Wait For Continue bit in the Message Status register (see section **3.8.11 Message Status Register** on page 3-21). Use the Wait For Continue bit to find out when the module has arrived at the halted instruction block. When the module detects that the Halt bit (Continue Mode) has been reset, the module will reset the Wait For Continue bit in the Message Status Register and continue BC operation.

The Halt operation can be implemented only in message blocks that have *not* yet been executed by the module.

Note: The Halt operation can be used in conjunction with the Jump command described below. See **3.2.9 Jump Command Operation** on page 3-8.

3.2.8 Skip Message

The Skip Message command allows the user to skip a message defined in a certain message block. To do so, modify the Command field in the Control Word. This lets the user selectively send a message in the current frame. The 'skip' takes place immediately and does not wait until the Intermessage Gap Time expires.

Note: The Control Word for the following message is processed during end of message processing for the current message. Therefore, performing a Skip or Restore (undoing the Skip) cannot be done during the Intermessage Gap Time preceding the message to be skipped or restored.

3.2.9 Jump Command Operation

The module's BC transfer cycle can be modified by setting the Jump command in the BC Control word. The Jump command instructs the module to operate on a new instruction stack or new stack entry in the same stack. This Control word is followed by a Stack Pointer word instead of the usual 1553 command word. In addition, the stack pointer is followed by an Instruction Count value. The Jump command is tested *after* the module has tested the Halt/Continue bit in the Control word. The 'jump' takes place immediately and does not wait until the Intermessage Gap Time expires.

The memory structure of the jump command is illustrated below.

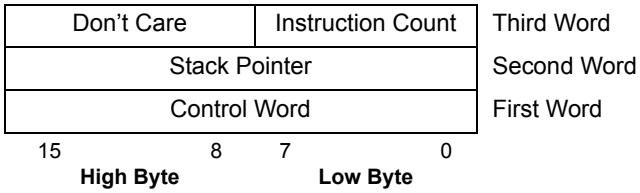


Figure 3-4 Jump Command Memory Structure

3.2.10 Minor Frame Operation

The Minor Frame type of message can be used in the following ways:

- To function as a "delay time" message between groups of messages.
- To produce a list of messages that will be sent out over the bus at different frequencies.

Minor frame time is defined as the time elapsed from the beginning of a minor frame to beginning of the next minor frame. To set up minor frame operation, each minor frame must begin with a minor frame command (see **Minor Frame Time Register** and **Minor Frame Time Multiplier Register** on page 3-25). The maximum value possible for the Minor Frame Time is 800 milliseconds.

The example Figure 3-5 **Minor Frame Sequencing** shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 msec. long, Message A is sent every 10 msec., Message B is sent every 20 msec., and Message C is sent every 40 msec.

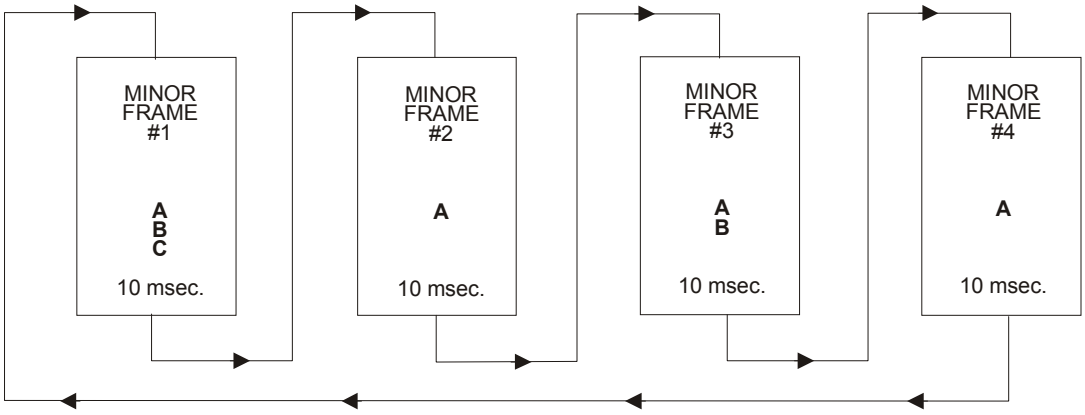


Figure 3-5 Minor Frame Sequencing

Notes:

1. The MINOR_FRAME message does not appear as a real message on the data bus.
2. Frame Time should not exceed the total time of all the minor frames in the minor frame sequence (see **Frame Time Multiplier Register** on page 3-24).

3.2.11 Asynchronous Frame Operation

During standard operation, the module sets up a frame of messages and then sends them out synchronously over the bus. The user can set up multiple frames of messages, and select which one to send out.

Asynchronous Frame operation allows the user to transmit a frame asynchronously. This means that in the middle of the transmission of the messages of a frame (frame 1), another frame (frame 2) can be transmitted, and then returned to continue transmitting the messages of the previous frame (frame 1).

To transmit an asynchronous frame, the user must write the number of messages in the asynchronous frame into the Asynchronous Message Count register, place a pointer to the beginning of the asynchronous frame in the Asynchronous Frame Pointer register, and then set the Asynchronous Start Flag register to a non-zero value. This will send out the asynchronous frame over the bus (see **Asynchronous Start Flag Register**, **Asynchronous Frame Pointer Register** and **Asynchronous Message Count Register** on page 3-29).

3.3 Remote Terminal Simulation

When the module is simulating both the Bus Controller and one or more Remote Terminals, the user must write the simulated Remote Terminal 1553 Status word and Data Word(s) into the message block in the sequence in which they are to be transmitted over the 1553 bus (see section **3.4 Message Block Formats** on page 3-12).

To indicate to the module, which Remote Terminals are to be simulated, write to the 32- byte Active Remote Terminal table. Each entry in the 32-byte table corresponds to a specific Remote Terminal.

The first byte is for RT #0, the second to RT #1, and the last byte is for RT #31 (for a total of 32 locations). A table entry value of 1 enables the Remote Terminal simulation by the module; a value of 0 disables the simulation by the module.

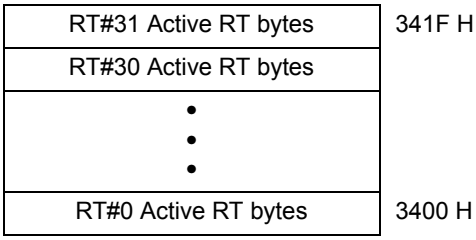


Figure 3-6 Active RT Table: BC/Concurrent RT mode

Bit	Description
01–07	Reserved – set to 0
00	1 Enabled 0 Disabled

Active RT Byte Definition: BC/Concurrent RT mode

3.4 Message Block Formats

The Message block contains, or will contain after response from an RT, the entire 1553 message as it appears on the 1553 bus, including Command word(s), Data Word(s), and Status word(s).Examples of Message block formats follow.

Example No. 1: Transmit Command Operating as BC Only

Block *before* execution

1553 Transmit Command	
Control Word	First Location in Block

Block *after* execution

1553 Data Word	First Transmitting Remote Terminal (not simulated)
•	•
•	•
1553 Data Word	•
RT Status Word	First Transmitting Remote Terminal (not simulated)
1553 Transmit Command	
Control Word	First Location in Block

Example No. 2: Receive Command Operating as Both BC and Receiving RT

Block *before* execution

RT Status Word	Simulated by M4K1553Px (Loaded by user)
1553 Data Word	•
•	•
•	•
1553 Data Word	Simulated by M4K1553Px (Loaded by user)
1553 Receive Command	
Control Word	First Location in Block

Block *after* execution

RT Status Word	
1553 Data Word	
•	
•	
1553 Data Word	
1553 Receive Command	
Control Word	First Location in Block

Example No. 3: RT-to-RT Command Operating as BC and Receiving RT

Block *before* execution

(Receive) RT Status Word	Simulated by M4K1553Px (Loaded by user)
Leave empty for Data +N	
•	
•	
Leave empty for Data #1	
Leave empty for (transmit) RT Status Word	
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location in Block

Block *after* execution

(Receive) RT Status Word	
1553 Data Word	From transmitting Remote Terminal (not simulated)
•	•
•	•
1553 Data Word	•
(Transmit) RT Status Word	From transmitting Remote Terminal (not simulated)
1553 Transmit Command	
1553 Receive Command	
Control Word	First Location in Block

Figure 3-7 Message Block Formats

3.5 Continuous or One-Shot Message Transfers

The module can transfer all programmed messages once, in a continuous loop, or for *n* number of times.

One-shot mode In One-Shot mode, after receiving a Start command, the module transfers all messages, sets the Message Complete bit in the Message Status register, issues an interrupt (if programmed), turns off bit 00 of the Start Register, and waits for a new Start command. Use the **Start Register** on page 3-20, to select One-Shot mode.

n-Times mode In n-Times mode, load the Loop Count register with the number of times to transmit the messages (frame) and set the Loop and Start bits in the Start register. The user can transmit messages from 1 to 255 times. (See **Start Register** on page 3-20 and **Loop Count Register** on page 3-22.) The **Frame Time Registers**, on page 3-24, determine the time between frames.

Continuous Loop mode In Continuous Loop mode, the module will retransmit the message frame at a predetermined, user-programmable rate. Use the **Start Register** on page 3-20 and **Loop Count Register** on page 3-22, to select Continuous Loop mode. In Continuous Loop mode, all messages relating to the (active) Stack pointer and Instruction counter are continuously looped until you halt the module's operation by clearing bit 00 of the Start register.

The Loop time or Frame time is a function of two control registers, the Frame Time Multiplier register and the Frame Time Resolution register. The internal Frame Time is loaded when a Start command is received. After all instructions are executed (1 frame), the module waits until the internal Frame Time counts down to 0 before reloading the Frame Time and transmits the next frame.

Note: If the Frame Time is less than the time required to transmit all messages within 1 frame, the subsequent frames will be transmitted with the minimum delay between them. The minimum delay is approximately 20 μsec, measured as dead time on the bus.

The Frame Time is composed of the Frame Time Resolution multiplied by the Frame Time Multiplier + 1.

The Frame Time Resolution register has a precision of 155 nanoseconds per bit.

Therefore, the maximum resolution is:

$$155 \times \text{FFFF (65535)} = 10157925 \text{ nanoseconds or } 10158 \text{ microseconds.}$$

The following algorithm first calculates the minimum Frame Time Multiplier and finds the appropriate resolution.

$$\text{frametime\_multiplier} = \frac{\text{desired time in microseconds}}{\text{10158 microseconds}}$$

$$\text{frametime\_resolution} = \left(\frac{\text{desired time in microseconds}}{\text{frametime\_ multiplier+1}} \times 1000\right) \Big/ 155$$

Example: To calculate a Frame Time of 500 msec.

500 milliseconds = 500000 microseconds

$$\text{frametime\_multiplier} = \frac{500000}{10158} = 49$$

$$\text{frametime\_resolution} = \left(\left(\frac{500000}{49+1} \times 1000\right) / 155\right) = 64516$$

Frame Time Resolution = 64516 Dec [FC04 H]

Frame Time Multiplier = 50 Dec [0031 H]

Before issuing the Start command, set:

- The Frame Time Multiplier register to 0031 H
- The Frame Time Resolution register to FC04 H

For descriptions of these registers see **Frame Time Multiplier Register** and **Frame Time Resolution Register**, on page 3-24.

3.5.1 Mode Codes

The module handles all dual-redundant 1553B mode codes; the Word count field is decoded according to MIL-STD-1553B. The module does not implement the two Quad-redundant mode codes, Selected transmitter Shutdown and Override Selected transmitter Shutdown.

3.6 1760 Header Word

1760 Options only

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header Word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first Data Word of the message.

The 1760 option provides predefined values, and these are preset on the *M4K1553Px* module.

For descriptions of the **1760 Header Value Table** and **1760 Header Exist Table** see page 3-26.

3.7 Program Example: BC/Concurrent-RT Modes

All values are in Hex unless otherwise stated.

BASIC Instruction	Remarks
`10 POKE &H3FFF,04`	Set the Configuration register to BC/RT mode.
`20 POKE &H3FF0,00`	Set the Stack Pointer registers to 0000.
`30 POKE &H3FF1,00`	(stack now begins at address: 0000)
`40 POKE &H3FF2,&HFF`	Set the Variable Amplitude register.
`50 POKE &H00,00`	Pointer to first message:
`60 POKE &H01,01`	[Location of message is 0100 (H)]
`70 POKE &H02,xx`	Set the Intermessage Gap Time location.
`80 POKE &H03,xx`	
`90 POKE &H08,&H40`	Pointer to second message:
`100 POKE &H09,01`	[Location of message is 0140 (H)]
`110 POKE &H0A,xx`	Set the Intermessage Gap Time location.
`120 POKE &H0B,xx`	
`130 POKE &H100,&H80`	Set the Control word to Transmit command,
`140 POKE &H101,00`	Bus A, and no errors injected.
`150 POKE &H102,&H23`	Set the Command word to 0C23.
`160 POKE &H103,&H0C`	
`170 POKE &H104,&H00`	Set the Status word to 0800.
`180 POKE &H105,&H08`	
`190 POKE &H106,&Hxx`	Set the Data Word to xxxx.
`200 POKE &H107,&Hxx`	
`210 POKE &H108,&Hyy`	Set the Data Word to yyyy.
`220 POKE &H109,&Hyy`	
`230 POKE &H10a,&Hzz`	Set the Data Word to zzzz.
`240 POKE &H10b,&Hzz`	
`250 POKE &H140,02`	Set the Control word to RT-to-RT command,
`260 POKE &H141,00`	Bus B, and no errors injected.
`270 POKE &H142,&H23`	Set the first (Receive) command word to 3823H.
`280 POKE &H143,&H38`	
`290 POKE &H144,&H43`	Set the second (Transmit) Command word to 1C43H.
`300 POKE &H145,&H1C`	
`310 POKE &H3FEB,2`	Set the Instruction Counter to 2 (i.e., 2 messages)
`320 POKE &H3FEC,xx`	Set the Frame Time Resolution register.
`330 POKE &H3FED,xx`	
`340 POKE &H3FEE,xx`	Set the Frame Time Multiplier register
`350 POKE &H3FEF,XX`	
`360 POKE &H3401,1`	Enable RT #1. Use the Active RT's look-up table to enable RTs. Module will simulate enabled RTs.
`370 POKE &H3FFC,1`	Set the Start register to 1. Starts message transfers in One-Shot mode.
`380 STOP`	

Program Example: BC/Concurrent-RT mode

3.8 Control Register Definitions

3.8.1 Additional Memory Area

Address: 7100–FFFF (H)

This area is available to the programmer for additional Instruction Stacks and Message Blocks

3.8.2 Time Tag Counter

Address: 7008–700B (H)

Read only

The user may read the current free-running, 32-bit Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first Lo word, then Hi word.

The counter is reset upon power-up or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting.

The counter must be read in the following sequence:

1. Read 7008 H (16 bit, read only)
2. Read 700A H (16 bit, read only)

7008 H contains the Lo word; 700A H contains the Hi word. The Time Tag resolution register sets the resolution of the counter.

3.8.3 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset register to reset the module's Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

Note: The counter is also reset from an external source. See section **7.4.2 Connector Pin Assignments: Px Configuration** on page 7-4.

3.8.4 Options Select Register

Address: 7003 (H)

Write only

Write to the Options Select register to select whether RT address 11111 (RT #31) is interpreted as a valid RT address or as a Broadcast address.

Bit	Description	
02-07	Don't Care	
01	Reserved	
00	1	Broadcast option is active. RT#31 is Broadcast Address. No RT Status Word will be transmitted.
	0	Broadcast option is inactive, RT#31 is a regular RT.

Options Select Register

Note: The Options Select register is reset at power-up (all bits set to 0). This register is not affected by a software rest and can be modified at any time without having to start and stop module operation.

3.8.5 Software Reset Register

Address: 7000 (H)

Set the Software Reset register to reset the module (data field = don't care)

Bit	Description
00-07	Don't Care

Software Reset Register

Note: Software Reset erases all locations in the dual-port RAM, module status, module ID and Firmware registers are written by the module after the reset operation is completed.

3.8.6 Module Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration register. To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20.)

Hex Value	Operating Mode
04	BC/Concurrent-RT

Module Configuration Register Value: BC/RT Mode

3.8.7 Module ID Register

Address: 3FFE (H)

The Module ID register contains a fixed value that can be read by your initialization function to detect the presence of the module. The one-byte value of this register is 45 (H), ASCII value E.

3.8.8 Module Status Register

Address: 3FFD (H)

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected, as described below. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Module Type is M4K1553Px
06	X (Don't Care)
05	X (Don't Care)
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit is cleared in the Start Register. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

3.8.9 Start Register

Address: 3FFC (H)

The Start register controls the Start/Stop operation of the module. Writing the appropriate bit (bit 00) to the Start register starts the Bus Controller transfer operation. When operating in Continuous Loop or *n*-Times mode, the user must set the Start and Loop bits in the Start register. The Loop and *n*-Times number are selected via the Loop Count register. In the One-Shot and *n*-Times modes, the module resets the Start bit in the register after *all* messages have been transferred. The module does not reset any bit while in Continuous Loop mode. To halt the Loop operation between messages, set bit 00 to 0. In order to halt the operation at the end of the entire frame, set bit 02 to 0 (bit 02 is not tested between message transfers). Related data bit 04 in the Module Status register indicates when the module has been halted. (See **Module Status Register** on page 3-19)

Bit	Description
03-07	0
02	1 = Loop Mode 0 = One-Shot Mode
01	0
00	1 = Start Operation 0 = Stop

Start Register

Note: The user can start concurrently by sending a low TTL pulse of 100nsec. minimum to the EXSTARTn pin, see section **7.4 Connectors** on page 7-3.

3.8.10 Interrupt Condition Register

Address: 3FFB (H)

The Interrupt Condition register allows the user to set interrupt triggers. When a condition occurs that is enabled in this register, an interrupt is generated. A logic 1 enables the interrupt condition. To determine which condition caused the interrupt, check the Message Status register.

The Interrupt Condition register must be set before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, and then issue a Start command. (**Start Register** on page 3-20).

Bit	Description
05-07	0
04	End Minor Frame
03	Message Error
02	End of Frame
01	Message Complete
00	0

Interrupt Condition Register

Note: The interrupt will be sent at the end of the message for all interrupt conditions.

3.8.11 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. The definition of each status bit is given below. Logic 1 indicates that the condition is activated.

Bit	Bit Name	Description
05-07	**Reserved**	Set to 0
04	**End Minor Frame**	A Trigger generated an interrupt on End of Minor Frame
03	**Message Error**	The message has been sent. As a result, the Error bit has been set in the Message Status word.
02	**End Of Frame**	The last word of the last message in the frame has been sent.
01	**Message Complete**	The last word of the message has been sent.
00	**Wait For Continue**	A message with the Halt bit set has been encountered. Reset the Halt bit in the Control word to continue.

Message Status Register

Note: Status bits are *not* reset by the module. After reading them, the user must reset them.

3.8.12 RT Response Time Register

Address: 3FF9 (H)

The RT Response Time register sets the Response Time of the Remote Terminal. The resolution of the Response Time register is 155 nsec. per bit. The minimum time is approximately 4 μsec., which is achieved by writing a 0 to this register. Any value above zero will result in a Response Time equal to 4 μsec. plus the contents of the register x 155 nsec. The actual response time has a tolerance of ± 1 μsec.

The Response Time register must be set before issuing a Start command to the module. To modify the RT Response Time register, issue a Stop command, modify the register, and then issue a Start command. (**Start Register** on page 3-20).

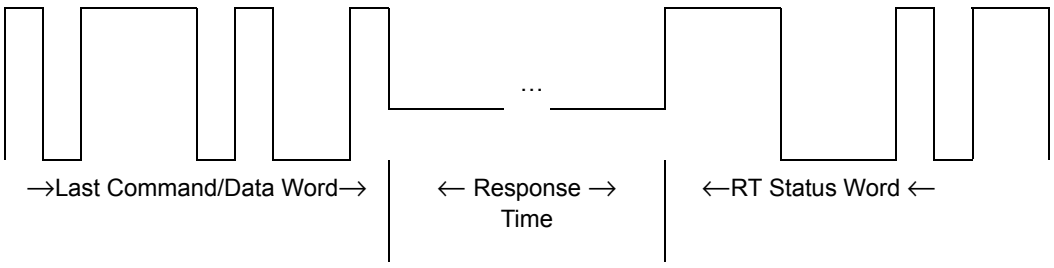


Figure 3-8 RT Response Time Definition

Example: To request a Response time of 9 μsec:
Write 32 to the RT Response Time Register
$32 \times 0.155 \cong 5$ μsec + 4 μsec = 9 μsec

3.8.13 Loop Count Register

Address: 3FF6 (H)

The Loop Count register is used in conjunction with the Loop bit in the Start register. If the Loop bit in the Start register is set, then set the Loop Count register to specify the number of times the Message frame will be transmitted. A value of zero is interpreted as a request for continuous looping. The Loop Counter register must be set before issuing a Start command to the module. To modify the Loop Counter register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20).

Bit	Value	Description
00-07	**0**	Transmits in Continuous Loop.
	1–255	Sends Message Frame n-times (1–255) as defined.

Loop Count Register

3.8.14 Bit Count Register

Address: 3FF5 (H)

The Bit Count register sets the total number of bits in the 1553 word, including Sync(3) and Parity(1). This register is used by the module only for messages for which the Bit Count Error bit is set in the Control Word of the Message Block (see section **3.2.6 Control Word** on page 3-7). If, the Bit Count Error bit is not set, a (valid) 20-bit word is transmitted regardless of the contents of the Bit Count register.

Set the Bit Count register before issuing a Start command to the module. To modify the Bit Count register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20).

Bit	Description			
03-07	**0**			
00-02	**Bit 02**	**Bit 01**	**Bit 00**	**No. of 1553 bits sent per word**
	0	0	0	17 (-3)
	0	0	1	18 (-2)
	0	1	0	19 (-1)
	0	1	1	20
	1	0	0	21 (+1)
	1	0	1	22 (+2)
	1	1	0	23 (+3)

Bit Count Register

3.8.15 Word Count Register

Address: 3FF4 (H)

The Word Count register controls the number of 1553 Data Words (±3) in the message and allows the user to inject a Word Count error. The error is an offset relative to the 1553 Command Word Word Count field. This register is used by the module only for messages for which the Word Count Error bit is set in the Control word register. (See **3.2.6 Control Word** on page 3-7). If the Word Count Error bit is not set, a correct number of words is transmitted regardless of the contents of the Word Count register.

The Word Count register must be set before issuing a Start command to the module. To modify the Word Count register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20).

Register Value	Word Count Offset
FD H	–3 Words
FE H	–2 Words
FF H	–1 Word
00 H	No Error Injection
01 H	+1 Word
02 H	+2 Words
03 H	+3 Words

Word count Register Values

3.8.16 BC Response Time Register

Address: 3FF3 (H)

The BC Response Time register sets the BC's Response Time window, whose value determines the maximum wait time until an RT's Status Response is considered invalid by the BC. The resolution of the BC Response Time register is 155 nsec. per bit, The minimum time is approximately 2 μsec.

The BC Response Time register must be set before issuing a Start command to the module. To modify the BC Response Time register, issue a Stop command, modify the register, and then issue a Start command. (**Start Register** on page 3-20).

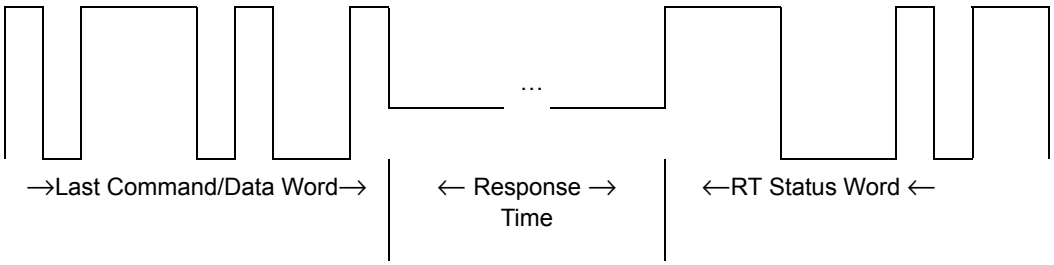


Figure 3-9 BC Response Time Definition

Example: To request a Response time of 14 μsec:
Write 90 to the BC Response Time Register
$90 \times 0.155 \cong 14$ μsec

3.8.17 Variable Amplitude Register Address: 3FF2 (H)

The Variable Amplitude register specifies the amplitude of the 1553 output signal. The signal can be programmed from 0 volts to 7.5 volts (peak-to-peak) when measured on the 1553 bus using 1553 direct coupling and 35-Ohm load (that is, two 70-Ohm termination resistors). If 78-Ohm termination resistors are used, a higher transmit (output) amplitude will appear on the 1553 bus. The Variable Amplitude register has a resolution of 30 mV/bit (p-p) on the bus.

Set the Variable Amplitude register before issuing a Start command to the module. To modify the Variable Amplitude register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20). After a reset, the Variable Amplitude register defaults to FF (H), providing maximum amplitude.

3.8.18 Stack Pointer Address: 3FF0–3FF1 (H)

The Stack pointer points to the Instruction stack. The Instruction stack can reside anywhere between the locations 0000 (H) and 33FF (H). The Stack Pointer register must be set before issuing a Start command to the module. To modify the Stack Pointer register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20).

3.8.19 Frame Time Multiplier Register Address: 3FFE–3FEF (H)

The Frame Time Multiplier register contains the 16-bit Frame Time value for Continuous and *n*-Times modes operation. The value written to the Frame Time Multiplier register is multiplied by the value set in the Frame Time Resolution register described below. The value set must equal the desired multiplication factor -1.

See **Example: To calculate a Frame Time of 500 msec.** on page 3-15

The Frame Time Multiplier register must be set before issuing a Start command to the module. To modify the Frame Time Multiplier register, issue a Stop command, modify the register, then issue a Start command. (See **Start Register** on page 3-20).

3.8.20 Frame Time Resolution Register Address: 3FEC–3FED (H)

The 16-bit Frame Time Resolution value represents the resolution of the Frame Time counter in increments of 155 nsec. (See section **3.5 Continuous or One-Shot Message Transfers** on page 3-14.)

The Frame Time Resolution register must be set before issuing a Start command to the module. For an example of how to calculate Frame Time Multiplier and Frame Time Resolution, see Calculating Frame Time, page 3-15. To modify the Frame Time Resolution register, issue a Stop command, modify the register, then, issue a Start command. (See **Start Register** on page 3-20).

3.8.21 Instruction Counter

Address: 3FEB, 3FEA (H)

The Instruction Counter must be loaded with the number of instructions (1553 Messages) to execute in the current frame. The value must be greater than 0 before the user writes to the Start register to begin a transmission. Set the Instruction counter to 1 for one message, 2 for two messages, etc. The module updates the Instruction counter by decrementing the value and writing it back to memory at the end of each message transfer.

The Instruction Counter register must be set before issuing a Start command to the module. To modify the Instruction Counter register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20). When in Continuous Loop mode, the Instruction Counter register cycles from the initial value down to 1.

The low register [3FEA] contains the MSB; the high register [3FEB] contains the LSB. Therefore, for an Instruction Counter less than 256, use the LSB only, address 3FEB.

3.8.22 Minor Frame Time Register

Address: 3FE8–3FE9 (H)

Write only

This 16-bit Minor Frame Time register is used to set the length of a single minor frame. (See section **3.2.10 Minor Frame Operation** on page 3-9.) The resolution of the Minor Frame Time register is 1 μsec. per bit. The maximum value is approximately 65 msec., which can be extended by the multiplier set in the Minor Frame Time Multiplier register.

The Minor Frame Time register must be set before issuing a Start command to the module. To modify the Minor Frame Time register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20.)

3.8.23 Minor Frame Time Multiplier Register

Address: 3FE6–3FE7 (H)

Write only

The Minor Frame Time Multiplier register is a multiplier of the Minor Frame Time register described above. The value written by the user to the Minor Frame Time Multiplier register allows the user to extend the Minor Frame Time beyond the 65 msec. maximum in the Minor Frame Time register. The maximum Minor Frame Time Multiplier is 255. The maximum Minor Frame Time possible using both registers is approximately 800 milliseconds.

Example: To generate a Minor Frame Time of 1 sec., set the Minor Frame Time register to F424 (H) [62,500 Dec.], and set the Minor Frame Time Multiplier register to 10 (H) [16 Dec.].

The Minor Frame Time Multiplier register must be set before issuing a Start command to the module. To modify the Minor Frame Time Multiplier register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 3-20).

3.8.24 Replay Register

Address: 3FE5 (H)

The Replay Register, if set to 1, indicates that the module uses the Intermessage Gap Time (IMG) field as a Time Tag (TTAG) indicator. Instead of reading the IMG field to determine how much time to allow for the intermessage gap, the module reads it as the Time Tag value used for the start time of the next message. When the message completes, the following steps are taken until step 2b. is executed successfully:

1. The module computes the:

TIME_DELTA	=	Real Time Tag (taken from the Time Tag registers at 7008–700B H)	–	Intermessage Gap Time

2a. If TIME_DELTA is > 0 Go to step 1

2b. If TIME_DELTA is < = 0 The module immediately sends out the next message

The Replay register can be used to reconstruct a previously recorded data run. The module will transmit the same data on the bus, using the recorded Time Tag as the time to send out the message, instead of using the Intermessage Time Gap.

3.8.25 1760 Header Value Table

Address: 3F40–3F7F (H)

1760 Options only

Write to the 1760 Header Value table to set the value you expect to receive in the first Data Word of the RT-to-BC or RT-to-RT message.

The 1760 option provides predefined values, and these are preset on the *M4K1553Px* module. The user can change the preset values.

Address	Hex Value	Associated Subaddress
3F42 H	0421	1
3F56 H	0420	11
3F5C H	0423	14

Transmit Subaddress: BC/Concurrent-RT mode

3.8.26 1760 Header Exist Table Address: 3EC0–3EFF (H)

1760 Options only

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for RT-to-BC or RT-to-RT messages directed to that Subaddress.

For those Header Value Table entries for which MIL-STD-1760 provides predefined values, the corresponding Header Exist Table entries are preset on the *M4K1553Px* module.

To set other values, enable the Header Exist Table entry for this RT (set it to 1) and write the value to the Header Value Table.

Bit	Description
09-15	Reserved
08	1 = Module should expect a Header word 0 = Module should **not** expect a Header word
00-07	Reserved

1760 Header Exist Table

Address	Hex Value	Associated Subaddress
3EC2 H	0100	1
3ED6 H	0100	11
3EDC H	0100	14

Transmit Subaddress: BC/Concurrent-RT mode

3.8.27 Send Time Tag on Sync Register Address: 3E8A–3E8B (H)

Set the Send Time Tag on Sync Register to indicate that the module should send the current Time Tag value (with a resolution of 64 μsec.) as the 16-bit Data Word upon transmitting a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

3.8.28 Clear Time Tag on Sync Register Address: 3E88–3E89 (H)

Set the lower bit [3E88 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag Registers [7008–700B H] (reset to 0) upon the transmission of a Mode Code 1 message (synchronize). A value of 0 disables this function.

Set the higher bit [3E89 H] of the Clear Time Tag on Sync Register to indicate that the module should clear the Time Tag Registers [7008–700B H] (reset to 0) upon the transmission of a Mode Code 17 message (synchronize with data). A value of 0 disables this function.

3.8.29 Module Options Register

Address: 3E84–3E85 (H)

Read only

The Module Options register is a 16-bit register that identifies the type of on-module firmware.

Bit	Description	
15	Reserved	
14	'1' M4KPx	
10–13	Reserved	
09	'1' 1760	
08	'1' 1553	
00–07	Module Type	4D H = PMx module 50 H = Px module

Module Options Register

3.8.30 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-module firmware. The value 0001 0010 would be read as revision level: 1.2.

3.8.31 Asynchronous Start Flag Register

Address: 3424–3425 (H)

Write only

To indicate that it is now time to send a selected frame asynchronously, write a 1 to the Asynchronous Start Flag register. The module will automatically reset this value to 0 when it sends the frame.

3.8.32 Asynchronous Frame Pointer Register

Address: 3422–3423 (H)

Write only

To send asynchronously to this register, write the address at the beginning of the selected frame.

3.8.33 Asynchronous Message Count Register

Address: 3420–3421 (H)

Write only

Write the number of messages contained in the Asynchronous Frame. The maximum number of messages allowed in a frame is determined by the amount of available space in the message stack area of the module and the size of the individual messages

4 Bus Monitor Operation

Chapter 4 describes *M4K1553Px* operation in Bus Monitor mode. The topics covered are:

4.1 Sequential Fixed-Block Memory Map 4-3
4.2 Sequential Link-List Memory Map 4-4
4.3 Sequential Mode Message Block Area 4-5
4.4 Look-up Table Mode Memory Map 4-7
4.5 Look-up Table Mode 4-8
4.6 Look-up Table Mode Message Block Area 4-9
4.7 Message Status Word 4-10
4.8 Time Tag Word 4-12
4.9 1760 Header Word 4-12
4.10 Trigger Operation 4-13
4.11 Program Examples: Bus Monitor Mode 4-17
4.12 Control Registers Definitions 4-19

The Bus Monitor can operate in one of two modes:

Sequential mode: 1553 Message Blocks are stored in sequential locations in memory. Sequential mode supports two types of operations:

Fixed-block operation: 1553 messages are stored at fixed sequential blocks in the memory. Sequential Fixed Block mode supports Trigger capability

Link-list operation: 1553 messages are packed one after another in the memory, separated by a header.

Look-Up Table mode: Each 1553 message is stored in a unique Message Block. In Look-Up Table mode, the module addresses the user-programmable Look-up table when it receives a 1553 Command word. The Command word's RT address, T/R bit, and Subaddress fields make up the 11-bit pointer to a Look-Up table with 2048 (2K × 8) locations.

Use the **Module Configuration Register** on page 4-21, to program the desired mode of operation.

To determine if the module is installed and ready to operate:

Perform the following procedure after a power-up or a software reset.

1. Check the Module ID register (test for value = 45 H).
2. Check the Module Status register (test for Module Ready bit = 1).

The module is installed and ready when both registers contain the correct values (as written above). For software reset operations, set these values to 0 immediately prior to writing to the module Software Reset register.

Note: Throughout this manual, writing a 1 to the Start register is referred to as issuing a Start command.

4.1 Sequential Fixed-Block Memory Map

Figure 4-1 **Bus Monitor: Sequential Fixed-Block Memory Map** illustrates the Sequential Fixed-Block memory map.

Additional Memory Area (for future use)	7100–FFFF H		
Reserved	700C–70FF H		
Time Tag Counter Word 1	700A–700B H		
Time Tag Counter Word 0	7008–7009 H		
Time Tag Reset Register	7007 H		
Reserved	7004–7006 H	Trigger Mask #1	3FF0–3FF1 H
Options Select Register	7003 H	Trigger Word #2	3FEE–3FEF H
Reserved	7001–7002 H	Trigger Mask #2	3FEC–3FED H
Software Reset Register	7000 H	Trigger Control Register	3FEB H
Reserved	4000–6FFF H	Mode Code Control Register	3FEA H
Module Configuration Reg	3FFF H	Broadcast Control Register	3FE8–3FE9 H
Module ID Register	3FFE H	Reserved	3F80–3FE7 H
Module Status Register	3FFD H	1760 Header Value Table[1]	3F00–3F7F H
Start Register	3FFC H	1760 Header Exist Table[1]	3EC0–3EFF H
Interrupt Condition Register	3FFB H	Reserved	3E90–3EBF H
Message Status Register	3FFA H	Monitor Response Time Reg.	3E8E–3E8F H
Reserved	3FF8–3FF9 H	Reserved	3E86–3F8D H
Time Tag Resolution Register	3FF7 H	Module Options Register	3E84–3E85 H
Reserved	3FF6 H	Reserved	3E81–3E83 H
Message Counter Register	3FF5 H	Firmware Revision Register	3E80 H
Counter Trigger	3FF4 H	Message Block Area(200 Blocks)	0000–3E7F H
Trigger Word #1	3FF2–3FF3 H		

Figure 4-1 Bus Monitor: Sequential Fixed-Block Memory Map

1. 1760 Options only

4.2 Sequential Link-List Memory Map

Figure 4-2 **Bus Monitor: Sequential Linked-list Memory Map** illustrates the Sequential Link-list Memory Map.

Additional Memory Area (for future use)	7100–FFFF H		
Reserved	700C–70FF H		
Time Tag Counter Word 1	700A–700B H		
Time Tag Counter Word 0	7008–7009 H		
Time Tag Reset Register	7007 H		
Reserved	7004–7006 H		
Options Select Register	7003 H		
Reserved	7001–7002 H		
Software Reset Register	7000 H	Mode Code Control Register	3FEA H
Reserved	4000–6FFF H	Broadcast Control Register	3FE8–3FE9 H
Module Configuration Reg	3FFF H	Reserved	3F80–3FE7 H
Module ID Register	3FFE H	1760 Header Value Table[1]	3F00–3F7F H
Module Status Register	3FFD H	1760 Header Exist Table[1]	3EC0–3EFF H
Start Register	3FFC H	Reserved	3E90–3EBF H
Interrupt Condition Register	3FFB H	Monitor Response Time Reg.	3E8E–3E8F H
Message Status Register	3FFA H	Reserved	3E86–3F8D H
Reserved	3FF8–3FF9 H	Module Options Register	3E84–3E85 H
Time Tag Resolution Register	3FF7 H	Reserved	3E81–3E83 H
Reserved	3FF6 H	Firmware Revision Register	3E80 H
End Point Buffer	3FF4–3FF5 H	Message Block Spill Area	3400–3E7F H
Next Message Pointer	3FF2–3FF3 H	Message Block Area (200 Blocks)	0000–33FF H
Reserved	3FEB–3FF1 H		

Figure 4-2 Bus Monitor: Sequential Linked-list Memory Map

1. 1760 Options only

4.3 Sequential Mode Message Block Area

The Sequential Mode Message Block area is partitioned into either blocks of fixed length or into a link-list of blocks of varying lengths. The **Module Configuration Register** on page 4-21, determines the type of partitioning.

For a description of the Time Tag function, see **4.8 Time Tag Word** on page 4-12.

4.3.1 Message Block Fixed-Block Operation

In Fixed-Block operation, the Message Block area is divided into 200 blocks of 80 bytes each. The first block starts at address 0000 (H), the second at 0050 (H), the third at 00A0 (H), etc. The Trigger option can be used only in Sequential mode with Fixed-Block operation. (See section **4.10 Trigger Operation** on page 4-13).

Information is stored in the memory in the following sequence	Byte offset
1553 Data Word	•
•	•
•	•
•	•
1553 Data Word	+8
1553 Command Word	+6
Time Tag Word 1	+4
Time Tag Word 0	+2
Message Status Word	0

Figure 4-3 Bus Monitor Message Block: Fixed-Block Operation

4.3.2 Message Block Link-list Operation

In Link-list operation, the Message Block area is divided into a linked list of message blocks. The length of each message block varies according to message size. The first two locations in each block comprise the message header. This header contains the address of the next Message Block header. The header of the last 1553 block received contains *xx*FF (End of File), indicating that there are no more messages stored. After a message is processed and stored in memory, the header of the preceding message block is updated from *xx*FF to the address (of the header in the block) of the newly stored message.

The Link-list method can store more data than Fixed-Block operation.

Take special care with the last message in the Message Block area. Since the buffer never wraps around in the middle of a message and a message may start at any address up to 3DFE (H), the final message in the buffer may extend past the end of the standard Message Block area into the Message Block Spill area. The End Buffer pointer (see **End Buffer Point** on page 4-25) exists for this special case. The End Buffer pointer points to the address after the last location of the message, indicating the length of the message. The next message will start at the first location of the Message Block area (0000 H).

The Figure 4-4 illustrates the contents of the Message block. For a description of the Time Tag function, see section **4.8 Time Tag Word** on page 4-12.

Information is stored in the memory in the following sequence:	Byte Offset
End Of File: XXFF	•
1553 Data Word	•
•	•
•	•
•	•
1553 Data Word	+A
1553 Command Word	+8
Time Tag Word 1	+6
Time Tag Word 0	+4
Message Status Word	+2
Message Header - Address of Next Block	0

Figure 4-4 Bus Monitor Message Block: Link-list Operation

4.4 Look-up Table Mode Memory Map

Figure 4-5 **Bus Monitor Look-up Table Mode Memory Map** illustrates the Look-up Table memory usage.

Additional Memory Area (for future use)	7100 – FFFF H		
Reserved	700C – 70FF H		
Time Tag Counter Word 1	700A – 700B H		
Time Tag Counter Word 0	7008 – 7009 H		
Time Tag Reset Register	7007 H		
Reserved	7004 – 7006 H		
Options Select Register	7003 H		
Reserved	7001 – 7002 H		
Software Reset Register	7000 H	Broadcast Control Register	3FE8–3FE9 H
Data Block Look-up Table (2K × 8)	4000 – 47FF H	Reserved	3F80–3FE7 H
Module Configuration Register	3FFF H	1760 Header Value Table[1]	3F00 – 3F7F H
Module ID Register	3FFE H	1760 Header Exist Table[1]	3EC0 – 3EFF H
Module Status Register	3FFD H	Reserved	3E90 – 3EBF H
Start Register	3FFC H	Monitor Response Time Reg.	3E8E–3E8F H
Interrupt Condition Register	3FFB H	Reserved	3E86 – 3F8D H
Message Status Register	3FFA H	Module Options Register	3E84–3E85 H
Reserved	3FF8 – 3FF9 H	Reserved	3E81 – 3E83 H
Time Tag Resolution Register	3FF7 H	Firmware Revision Register	3E80 H
Reserved	3FF1 – 3FF6 H	Reserved	2800 – 3E7F H
Last Block Register	3FF2 H	Message Block Area (128 Blocks)	0000 – 27FF H
Reserved	3FEB – 3FF1 H		
Mode Code Register	3FEA H		

Figure 4-5 Bus Monitor Look-up Table Mode Memory Map

1. 1760 Options only

4.5 Look-up Table Mode

In Look-up Table mode, the module can store 128 unique messages by using a 2K × 8 Look-up table in on-module memory. Each byte in the table is divided into a 7-bit block number and an Interrupt Select bit, as described below. Data Block numbers (0 - 127 decimal) each consisting of 80 bytes are loaded into the table. The first block starts at address 0, the second at 50 (H), etc. Set the Interrupt Select bit to specify which messages will set the interrupt flag. The Interrupt Condition register must also be programmed.

Bit	Description
07	1 Interrupt Select bit is enable
00–06	Block Numbers (0–127)

Look-up Table Byte Structure

When a 1553 message is received, the Command word's RT address, T/R Bit, and Subaddress fields are used as an 11-bit index to the look-up table. This index is used to extract the Data block number from the Look-up table.

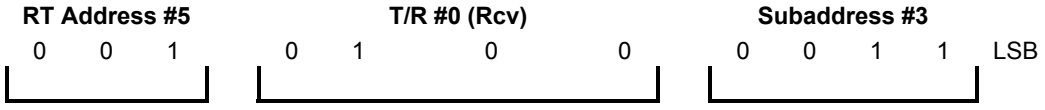
	11 most significant bits of the 1553 Command word					
Base Address	**RT address (5 bits)**	**T/R (1 bit)**	**Sub-address (5 bits)**	**Look-up table (2K x 8)**	**Data block**	**Hex address of Data Block**
4000+	11111	1	11111	Block #	Data Block 127	27B0
	•	•	•	•	•	
	•	•	•	•	•	
	•	•	•	•	•	
4000+	00000	0	00001	Block #	Data Block 3	00F0
4000+	00000	0	00010	Block #	Data Block 2	00A0
4000+	00000	0	00001	Block #	Data Block 1	0050
4000+	00000	0	00011	Block #	Data Block 0	0000

Figure 4-6 Look-up Table

To create the address to the table

1. Isolate the eleven (most significant) bits of the 1553 command word (RT Address, T/R, and Subaddress field), and determine their hex value.

Example: To allocate a data block for a 1553 receive message to RT#5, Subaddress #3.



Hex representation = 143 (H)

2. Add the hex value of this part of the command word to the base address of the look-up table (4000H).

```
  4000  (H)
+ 143   (H)
--------
  4143  (H)
```

3. Write the data block number to this location.

Example: **POKE&H4143**, writes an 8-bit Block number value to the Look-up table address **&H14143**. Each data block, beginning at address 0000 is 80 bytes long (for up to 32 1553 Data words). The address of a block is obtained by multiplying its block number by 50 (H).

The block addresses are calculated as follows:

- Block 0 is located at location 0000 (H).
- Block 1 is located at location 0050 (H).
- The location of the block is obtained by multiplying the block number by 50 (H).

4.6 Look-up Table Mode Message Block Area

Information is stored in the memory in the following sequence:	Byte Offset
See **Appendix B MIL-STD-1553 Message Formats** on page B-1	• • • •
1553 Command Word	+6
Time Tag Word 1	+4
Time Tag Word 0	+2
Message Status Word	0

Figure 4-7 Bus Monitor Message Block: Link-list Operation

4.7 Message Status Word

The Message Status word is identical for all Bus Monitor modes. The Message Status word indicates the status of the message transfer. The module creates this Word. Do not confuse it with the 1553 Status word. (See **1553 RT Status Words** on page 2-7). The contents of the Message Status word are described below.

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed.
14	**Trigger Found**	Trigger message was received and stored. This status is valid for Sequential Fixed-Block mode with the following modes: **Store After** mode: the Trigger Found bit will be set only in the *first* Trigger message. **Store Only** mode: the Trigger Found bit will be set in *every* Trigger message. (See **4.10 Trigger Operation** on page 4-13)
13	**RT-RT**	RT-to-RT message was received.
12	**Message Error Bit Set**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status Bit Set**	A bit other than the Message Error bit in the RT Status word was set. The Error Bit is *not* set in conjunction with this bit.
10	**Invalid Message**	1553 message-level error occurred (Word Count, Incorrect Sync, etc.). Examine the other bits in this table to determine which error occurred.
09	**Checksum Error**	The computed checksum (on the incoming message) does not match when checked against the last Data Word received. (See **1.1.2 MIL-STD-1760 Considerations** on page 1-3)
08	**Bus A / B**	Bus on which the message was transferred: 0 = Bus B 1 = Bus A
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity).
05-06	**Word Count/ Header Error**	**Bit 06** / **Bit 05** / **Description**: 0 / 0 / Reserved 0 / 1 / Word Count Low 1 / 0 / Word Count High 1 / 1 / 1760 Header Error – Header Word received does not match the value set in the Header Value Table.
04	**Incorrect RT Address**	Received 1553 Status word did not contain the correct RT address.
03	**Incorrect Sync Received**	Sync of either the command or the Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**Response Time Error**	Response Time error occurred in the message.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word

Note:

1. The Message Status Word is valid only when bit 15, End of Message, is turned on.
2. When the module completes receiving a message over the bus, it writes the Message Status Word for this message in its message storage location. The module then zeros out the Message Status Word in the next message storage location, in preparation for receiving the next message over the bus.

4.8 Time Tag Word

In all Bus Monitor modes, each incoming message is stored with a Time Tag value. The Time Tag value is a 32-bit word used to determine the time elapsed since the Start command was issued or the time between 1553 messages. The Time Tag uses a 32-bit, free running counter whose resolution is fixed at 4 µ sec. per bit. The Time Tag counter (to 0) may be reset at any time by writing to the Time Tag Reset register. (See **Time Tag Reset Register** on page 4-19)

The Time Tag counter's value is written to the dual-port RAM during the reception of the (first) command of each message.

Note: In addition to reading the Time Tag value in the message stack, you can also read the counter's value at any time in the Time Tag counter (See **Time Tag Reset Register** on page 4-19)

4.9 1760 Header Word

1760 Options Only

In the MIL-STD-1760 specification, the first Data Word of a message may be a Header Word, which is used for message identification. The Header word is associated with a specific RT subaddress.

To indicate that a specific subaddress will require a Header Word, set the corresponding entry in the 1760 Header Exist table to 1. Then set the corresponding entry in the 1760 Header Value table to the value you expect to receive in the first Data Word of the message.

The 1760 option provides predefined values. These are preset on the *M4K1553Px* module.

For descriptions of the **1760 Header Value Table** and **1760 Header Exist Table**, see page 4-27.

4.10 Trigger Operation

Only Sequential Fixed-Block mode supports triggers.

A trigger is a filter that the user can set to tell the module when and how to store 1553 messages. The module can be programmed to store messages in the following ways:

Store All	Stores all 1553 messages, without regard to triggers; no triggers are active
Store Only	Stores only messages that meet the trigger condition
Store After	Stores only the trigger message and messages that come after the trigger message

Up to two triggers may be defined. Each trigger is defined using two registers:

- **Trigger Word Registers (1 and 2)**
- **Trigger Mask Register (1 and 2)**

Use the Trigger Word register to define a particular 1553 Command word or a Message Status word as a trigger. For example, the user can use the Message Status word as the trigger source to store all messages on bus A, only messages with errors, or messages with errors received over bus B, etc. (See **Trigger Word Registers (1 and 2)** on page 4-14).

The Trigger Mask register defines which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ('don't care'). The Trigger Mask registers must be defined when using the trigger function. (See **Trigger Mask Register (1 and 2)** on page 4-15.)

Set the Trigger Control register to specify the following trigger conditions. (See **Trigger Control Register** on page 4-16):

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

The Trigger Word, Trigger Mask and Trigger Control registers must be set before issuing a Start command to the module. To modify these registers, set the Initialize bit in the Start register to 10 (H), modify the Trigger Word, Trigger Mask and Trigger Control registers, then issue a Start command 81 (H).

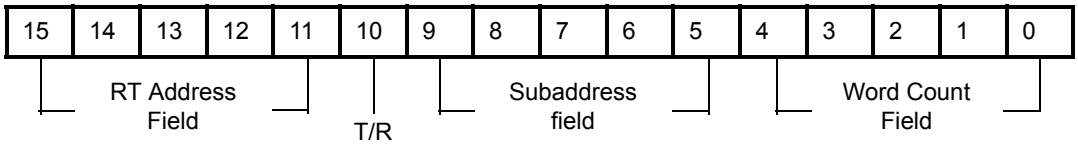
4.10.1 Trigger Word Registers (1 and 2)

Address: Word 1 3FF2–3FF3 (H)
Word 2 3FEE–3FEF (H)

Use the Trigger Word register to define a particular 1553 Command word or a Message Status word as a trigger. Load these locations (illustrated below) with the desired 1553 Command word or Message Status word, which will be used as the trigger source. The user must also define the Trigger Mask Registers when using the trigger function. (See **Trigger Mask Register (1 and 2)** on page 4-15). To define which trigger is to be active (Trigger #1, Trigger #2, or both) use the Trigger Control Register. (See **Trigger Control Register** on page 4-16).

USING THE 1553 COMMAND WORD: TRIGGER WORD REGISTERS

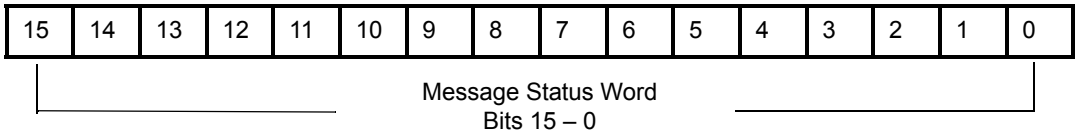
Use a 1553 Command word as a trigger when it is necessary to filter messages based on information found in the Command word. For example, to filter messages from a particular RT, or with a particular word count, set the Trigger Word register with those parameters defined in the 1553 Command word.



USING THE MESSAGE STATUS WORD: TRIGGER WORD REGISTERS

Use a Message Status word as a trigger when it is necessary to filter messages based on information found in the Message Status word. Do not confuse the Message Status word with the 1553 Status word (see **1553 RT Status Words** on page 2-7) to filter messages transferred over bus A (vs. bus B), or error messages, set the Trigger Word register with those parameters defined in the Message Status word.

For an explanation see **Message Status Word** on page 4-10.



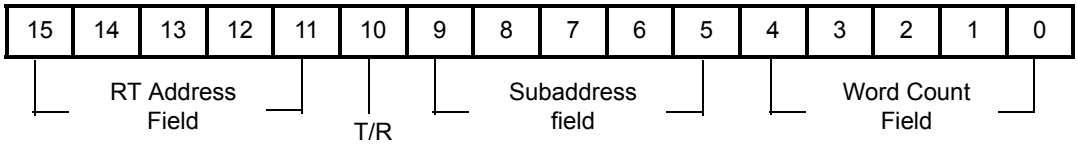
4.10.2 Trigger Mask Register (1 and 2)

Address: Word 1 3FF0–3FF1 (H)
Word 2 3FEC–3FED (H)

Set the Trigger Mask register to define which bits of the trigger word (defined in the Trigger Word register) are relevant and which can be ignored ("don't care"). The Trigger Mask registers must be defined when using the trigger function. All bits in this register should be set to 1, except for those bits you want to be "don't care" in the incoming Command word or Message Status word.

USING THE 1553 COMMAND WORD: TRIGGER MASK REGISTERS

After setting the Trigger Word register with a 1553 Command word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the 1553 Command word trigger.

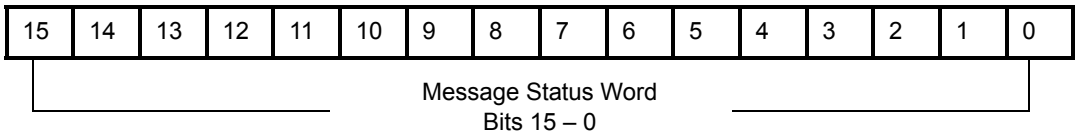


1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "Don't Care"

USING THE MESSAGE STATUS WORD: TRIGGER MASK REGISTERS

After setting the Trigger Word register with a Message Status word, write 0s to the bits in the Trigger Mask register that you want to be "don't care" in the Message Status word trigger.

For an explanation see **Message Status Word** on page 4-10.



1 = Trigger on corresponding bit value in Trigger Word Register
0 = Corresponding bit value in Trigger Word Register is "Don't Care"

4.10.3 Trigger Control Register

Address: 3FEB (H)

The Trigger Control register is relevant only in Sequential Fixed-Block mode. Set the Trigger Control register to specify the following trigger conditions:

- Trigger source (1553 Command word or Message Status word)
- Type of storage (Store All, Store Only, or Store After)
- Active trigger word (Trigger Word #1 and/or #2)

Note: Logic 1 enables the function.

Bit	Description
07	Trigger Source: 0 = 1553 Command Word 1 = Message Status Word
05-06	Reserved
04	1 = Store After
03	1 = Store Only
02	1 = Store All
01	1 = Enable Trigger Word #2
00	1 = Enable Trigger Word #1

Trigger Control Register

Example: Defining a Trigger

Conditions:

- Define the Command word 0825 (H) as Trigger word #1 (Receive Command for RT#1, Subaddress #1, and 5 words).
- Ignore the Word Count field.
- Use Trigger word #1 (Disable Trigger word #2).

Procedure:

1. Set Trigger Word #1 register to 0825 (H)
2. Set Trigger Mask #1 register to FFE0 (H)
3. Set Trigger Control register to 09 (H)

Note: To use trigger(s), at least one of the bits Store All, Store Only, or Store After, must be set.

4.11 Program Examples: Bus Monitor Mode

Bus Monitor Sequential Fixed-Block Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,08`	Set the Module Configuration register for Bus Monitor Sequential Fixed-Block mode.
`20 POKE &H3FF0,xx`	Set trigger mask #1- low to xx.
`30 POKE &H3FF1,xx`	Set trigger mask #1- high to xx.
`40 POKE &H3FF2,xx`	Set trigger word #1- low to xx.
`50 POKE &H3FF3,xx`	Set trigger word #1- high to xx.
`60 POKE &H3FEB,xx`	Set the Trigger Control register (see **Trigger Control Register** on page 4-16).
`70 POKE &H3FEA,00`	Set the Mode Code Control Register to 1s and 0s (see **Mode Code Control Register** on page 4-26).
`80 POKE &H3FE8,00`	Set the Broadcast Control register to RT31 = regular (see **Broadcast Control Register** on page 4-26).
`90 POKE &H3FFC,01`	Start command.

Bus Monitor Sequential Link-list Mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H10`	Set the Module Configuration register to Bus Monitor Link-List mode (see **Module Configuration Register** on page 4-21)
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (see **Mode Code Control Register** on page 4-26).
`30 POKE &H3FE8,01`	Set the Broadcast Control Register to RT31 = Broadcast (see **Broadcast Control Register** on page 4-26
`40 POKE &H3FFC,01`	Start command.

Note: In Sequential Fixed-block and Sequential Link-list mode, messages are read from the memory starting from address 0000.

Bus Monitor Look-up Table mode

BASIC Instruction	Remarks
`10 POKE &H3FFF,&H20`	Set the Module Configuration register to Bus Monitor Look-up Table
`20 POKE &H3FEA,00`	Set the Mode Code Control register to 1s and 0s (See **Mode Code Control Register** on page 4-26)
`30 POKE &H3FE8,00`	Set the Broadcast Control register to RT = 31
`40 POKE &H4143,00`	Set the Look-up Table so that the Command words and RT#5, Receive mode, and Subaddress 3 point to Data Block #0 (see **4.5 Look-up Table Mode** on page 4-8)
`50 POKE &H4144, 01`	Set the Look-up Table so that the Command words and RT#5, Receive mode, and Subaddress 4 point to Data Block #1 (see **4.5 Look-up Table Mode** on page 4-8)
`60 POKE &H3FFC, 01`	Start Command

Note: Messages are read from memory according to the address pointer derived from the Command word. See section **4.5 Look-up Table Mode** on page 4-8.

4.12 Control Registers Definitions

4.12.1 Time Tag Counter

Address: 7008–700B (H)

Read only

The user may read the current free-running, 32-bit Time Tag counter at any time. Read the two 16-bit words of the Time Tag counter value sequentially, first the Lo word, then the Hi word.

The counter is reset upon power-up, or software reset and stays reset until a Start command is issued. When a Start command is issued, the counter starts counting. To re-initialize to 0, write to the Time Tag Reset register. When it reaches the value FFFF FFFF (H), the counter wraps around to 0 and continues counting.

The counter must be read in the following sequence:

1. Read 7008 (H) (16 bit, read only)
2. Read 700A (H) (16 bit, read only)

Note: 7008 (H) contains the Lo word; 700A (H) contains the Hi word. The resolution of the counter is 4 μsec. per bit.

4.12.2 Time Tag Reset Register

Address: 7007 (H)

Write only

Write to the Time Tag Reset register to reset the Channel 1 Time Tag Counter (data field = don't care). Immediately after the reset, the counter will start to count from 0.

Note: The counter is also reset from an external source. See section **7.4.2 Connector Pin Assignments: Px Configuration** on page 7-4

4.12.3 Options Select Register Address: 7003 (H)

The Concurrent BM Control bit of the Options Select register is relevant only for users of the EXC-4000 family of boards with two, three or four *M4K1553Px* modules (P2, P3, P4).

The carrier board provides a second module (module#1 or module#3) which may be set up to operate as Concurrent Monitors on the 1553 bus connected to module#0 or module#2, accordingly. When configured in this way module#0 may operate as a BC and/or RT while module#1 will concurrently monitor the module#0 1553 bus. Similarly, module#2 may operate as a BC and/or RT while module#3 will concurrently monitor the module#2 1553 bus.

The Options Select register is used to select the bus to which module#1 or module#3 are connected. On reset module#1 and module#3 are set to monitor their own buses.

Module#0 and module#2 are always connected to their own 1553 buses in Monitor mode, independent of the state of this register.

OPTIONS SELECT REGISTER FOR MODULE#1: WRITE OPERATION

Bit	Description
02-07	Don't Care
01	Concurrent BM Control Bit: (only for /P2 or /P4 configurations) 1 = Select module#1 as Concurrent BM of module#0 0 = Select module#1 as Independent BM module
00	Set to 0

OPTIONS SELECT REGISTER FOR MODULE#3: WRITE OPERATION

02-07	Don't Care
01	Concurrent BM Control Bit: (only for /P4 configurations) 1 = Select module#3 as Concurrent BM of module#2 0 = Select module#3 as Independent BM module
00	Set to 0

Options Select Register: Write Operation

Note: The Options Select Register can be:

- modified at any time without having to start and stop the module operation
- reset at power-up (all bits set to 0). This register is not affected by a software reset.

4.12.4 Software Reset Register

Address: 7000 (H)

Set the Software Reset register to reset the module.

Bit	Description
00–07	Don't Care

Software Reset Register

Note: Software Reset erases all locations in the dual-port RAM, module status, module ID and Firmware registers are written by the module after the reset operation is completed.

4.12.5 Module Configuration Register

Address: 3FFF (H)

Before issuing a Start command to the module, set the operating mode of the module via the Module Configuration register. To modify the Module Configuration register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 4-23).

Hex Value	Operating Mode
08	BM Sequential Block
10	BM Sequential Link-list
20	BM Look-up Table

Module Configuration Register Values: Monitor Mode

4.12.6 Module ID Register

Address: 3FFE (H)

The Module ID register contains a fixed value that can be read by your initialization routine to detect the presence of the module. The one-byte value of this register is: 45 (Hex), ASCII value E.

4.12.7 Module Status Register

Address: 3FFD (H)

The Module Status register indicates the status of the module. In addition, this register indicates which options have been selected. Do not modify this register. Status bits are active if set to 1.

Bit	Description
07	1 = Module Type is M4K1553Px
05-06	X (Don't Care)
04	1 = Module Halted 0 = Module Running
03	1 = Self-Test OK
02	1 = Timers OK
01	1 = RAM OK
00	1 = Module Ready

Module Status Register

Note: Module operation stops after the Start bit in the Start Register is cleared. Following this, the module sets bit 04 (Module Halted). Certain registers may be modified only after the Module Halted bit has been set. After receiving a subsequent Start command (by writing to the Start register), the module resets the Module Halted bit. The condition of this bit after power-up or software reset is logic 1.

4.12.8 Start Register

Address: 3FFC (H)

The Start register controls the Start/Halt operation of the module.

Write to the Start register with the appropriate bit set to execute one of the functions described below.

Bit	Bit Name	Description
06–07	**Reserved**	Set to 0
05	**Stop on Trigger/ Continue**	This bit is used in **Sequential Fixed-Block mode only**. 1 = Stop On Trigger. Stop storing 1553 messages when the Message Counter equals the Message Counter Trigger. 0 = Continue After Stop. Continue monitoring operations. You must first set this bit to 1 before Halting the module (setting bit 00 = 0).
04	**Initialize Board**	Set this bit to re-initialize the module, in order to change the module's mode of operation (via the **Module Configuration Register** on page 4-21.) To switch Monitor modes, stop and start the module (Start/Halt bit (bit 00)) and set this bit (bit 04). After the specific function is completed, the module clears this bit and the Start/Halt bit to 0. Board Halted bit (04) of the Module Status register is set when both of the following are true: A Halt command is issued (bit 00 of this register is set to 0) An Initialize Board command is issued (this bit is set to 1) 1 = Initialize module 0 = Stay in Monitor Mode For more information see **Module Status Register** on page 4-22.
03	**Clear memory**	This bit clears the 1553 message blocks and all readable control registers. 1 = Clear Memory 0 = Don't Clear Memory
01–02	**Reserved**	Set to 0
00	**Start/Halt**	1 = Start Operation 0 = Halt Operation

Start Register

Note: The module tests Clear Memory (bit 03) and Initialize Board (bit 04) only when the Start/Halt bit (bit 00) = 0.

The user can start concurrently by sending a low TTL pulse of 100 nsec. minimum to the EXSTARTn pin. See section **7.4 Connectors** on page 7-3.

4.12.9 Interrupt Condition Register

Address: 3FFB (H)

Set the Interrupt Condition register to enable interrupt triggers. When a condition enabled in this register occurs, an interrupt is generated. Logic 1 enables the interrupt condition. Check the Message Status register to determine which condition caused the interrupt.

The Interrupt Condition register must be set before issuing a Start command to the module. To modify the Interrupt Condition register, issue a Stop command, modify the register, then issue a Start command (See **Start Register** on page 4-23).

Note: For all interrupt conditions, the interrupt will be sent at the end of the message.

Bit	Description
03-07	0
02	1 = Counter Trigger Match (Valid Only in Sequential Fixed-block mode)
01	1 = Message Reception in Progress (Valid in All Modes)
00	1 = Trigger Word Received (Valid Only in Sequential Fixed-block mode)

Interrupt Condition Register

4.12.10 Message Status Register

Address: 3FFA (H)

The Message Status register indicates the status of the current message being processed. Each status bit is described in the table below. Logic 1 indicates that the condition is activated.

Bit	Description
03-07	0
02	1 = Counter Trigger Match
01	1= Message Reception In Progress
00	1 = Trigger Word Received/Busy Trigger word received is valid only In Sequential Fixed-Block mode. Busy is valid in Linked-list and Look-up Table mode. The busy bit is set when the module is processing a message. It is set together with message reception in progress, but is reset approximately 5 msec. after the end of each message. For consecutive messages with short intermessage gap times, the busy bit may not be reset between messages.

Message Status Register

Note: Status bits are not reset by the module. They must be reset after reading them.

4.12.11 Time Tag Resolution Register — Address: 3FF7 (H)

The 8-bit value in the Time Tag Resolution register represents the resolution of the Time Tag Counter in units of 4 μsec.

To determine the Time Tag Counter's Resolution, use the following equation:

= (Time Tag Resolution register value + 1) × 4 μsec.

A value of 0 corresponds to a resolution of 4 microseconds; a value of 1 corresponds to a resolution of 8 microseconds, etc.

Set the Time Tag Resolution register before issuing a Start command to the module. To modify the Time Tag Resolution register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register,** page 4-23.)

4.12.12 Message Counter Register — Address: 3FF5 (H)

Sequential Fixed-block mode only

Read the Message Counter register to determine the current Message Block number (0–199). The value is incremented by the module as each message is received. The first counter increment (to 1), which indicates that the first message has been received and stored, occurs at the beginning of the *second* 1553 message transfer operation. To determine the arrival of the first 1553 message, check the Message Status word of the *first* Message block. The End of Message bit (bit 15) in the Message Status word will be set.

4.12.13 Counter Trigger Register — Address: 3FF4 (H)

Sequential Fixed-block mode only

Read the Counter Trigger register to determine when the module has updated a specific message block number. Set the Counter Trigger register to a value that when equal to the Message counter will set a bit in the Message status register and set an interrupt (if programmed in the Interrupt Condition register).

Set the Counter Trigger register before issuing a Start command to the module. To modify the Counter Trigger register, issue a Stop command, modify the register, and then issue a Start command. (See **Start Register** on page 4-23).

The module can be programmed to stop monitoring when the Counter Trigger value is equal to the Message Counter (see the Stop/Continue bit in the **Start Register** on page 4-23).

4.12.14 End Buffer Point — Address: 3FF4–3FF5 (H)

Link-list mode only

The End Buffer pointer points to the address following the last word in the final message in the Message Block area. The End Buffer pointer is updated each time a final message is written into the buffer. Final messages that are longer than the remaining available space in the Message Block area do not wrap around to the start of the buffer. They are spilled into the Message Block Spill area, which is contiguous to the Message Block area. The value of this register varies from 3400 (H) (end of Message Block area) to 347E (H) (end of Message Block Spill area). Until the first buffer wrap around occurs, this register contains 0000 (H)

4.12.15 Next Message Pointer

Address: 3FF2–3FF3 (H)

Link-list mode only

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 0 (H) to 33FE (H).

4.12.16 Last Block Register

Address: 3FF2 (H)

Look-up Table mode only

Read the Last Block register to determine the (Look-up Table) block number of the current 1553 message. This register is used to identify the location of the current 1553 message. The Last Block register is updated at the end of each message reception.

4.12.17 Mode Code Control Register

Address: 3FEA (H)

Set the Mode Code Control register to specify which 1553 Subaddress value indicates the reception of a 1553 Mode command.

The Mode Code Control register must be set before issuing a Start command to the module. To modify the Mode Code Control register, issue a Stop command, modify the register, then issue a Start command. (See the **Start Register** on page 4-23).

Bit	Description		
02-07	0		
00-01	**Bit 01**	**Bit 00**	**Subaddresses Recognized as Mode Code**
	0	0	31 and 0
	0	1	0
	1	0	31
	1	1	0 and 31

Mode Code Control Register

4.12.18 Broadcast Control Register

Address: 3FE8–3FE9 (H)

Set the Broadcast Control register to specify whether RT address 11111 should be regarded as a valid RT number or as the Broadcast address.

Bit	Description
01-07	0
00	1 = RT #31 is Broadcast Address 0 = RT #31 is Regular RT

Broadcast Control Register

4.12.19 1760 Header Value Table

Address: 3F00–3F7F (H)

1760 Options only

Write to the 1760 Header Value table to set the value expected to be received in the first Data Word of the message. The 1760 option provides predefined values. These are preset on the *M4K1553Px* module. The user can reset the preset values.

The first 32 words [3F00 – 3F3F (H)] are reserved for Header values associated with BC-to-RT messages. The second 32 words [3F40 – 3F7F (H)] are reserved for Header values associated with RT-to-BC and RT-to-RT messages.

Address	Hex Value	Associated Subaddress
3F16 H	0400	11
3F1C H	0422	14
3F42 H	0421	1
3F56 H	0420	11
3F5C H	0423	14

Transmit and Receive Subaddresses: Bus Monitor mode

4.12.20 1760 Header Exist Table

Address: 3EC0–3EFF (H)

1760 Options only

The 1760 Header Exist table contains 32 entries corresponding to 32 RT subaddresses. Each entry may be set to indicate whether, or not, the module should expect a header word for messages directed to that subaddress. In Bus Monitor Mode, there is a separate bit to select Header Words for transmit and receive messages.

For those Header Exist table entries for which MIL-STD 1760 provides predefined values, the corresponding Header Exist table entries are preset on the *M4K1553Px*. To set other values, enable the Header Exist table entry for this Subaddress (set it to 1) and write the value to the Header Value table.

Bit	Description
09-15	Reserved
08	1 = module should expect a Header word in a transmit message (RT-to-BC or RT-to-RT) 0 = module should **not** expect a Header word in a transmit message
01-07	Reserved
00	1 = module should expect a Header word in a receive message (BC-to-RT) 0 = module should **not** expect a Header word in a receive message

1760 Header Exist Table

Address	Hex Value	Associated Subaddress
3EC2 H	0100	11
3ED6 H	0101	14
3EDC H	0101	1

Transmit and Receive Subaddress: Bus Monitor Mode

4.12.21 Monitor Response Time Register

Address: 3E8E–3E8F (H)

The Monitor Response Time Register sets the maximum wait time until the Monitor considers an RT's Status Response valid.

The Monitor Response Time Register is measured in microseconds. The default value of the register is 14 μsec, if not set otherwise by the user.

4.12.22 Module Options Register

Address: 3E84–3E85 (H)

Read only

The Module Options register is a 16-bit register that identifies the type of on-module firmware.

Bit	Description	
15	Reserved	
14	'1' M4KPx	
10–13	Reserved	
09	'1' 1760	
08	'1' 1553	
00–07	Module Type	4D H = PMx module 50 H = Px module

4.12.23 Firmware Revision Register

Address: 3E80 (H)

The Firmware Revision register indicates the revision level of the on-module firmware. The value 0001 0010 would read as revision 1.2.

5 Internal Concurrent Monitor Option

Chapter 5 describes Internal Concurrent Monitor operation, an option available only on the *M4K1553PMx* module.

The following topics are covered:

5.1 Concurrent Monitor Memory Map 5-1
5.2 Message Block Area 5-2
5.3 Control Register Definitions 5-5

On the *M4K1553PMx* module the Concurrent Monitor operates automatically when the module is started in either RT or BC/RT modes. This monitor is not available when the module is not running in one of the above modes. It operates in sequential fixed block mode (the 1553 Message blocks are stored in sequential locations in memory). The storing of messages starts at the first block.

See **Chapter 8 Ordering Information** for part number details.

5.1 Concurrent Monitor Memory Map

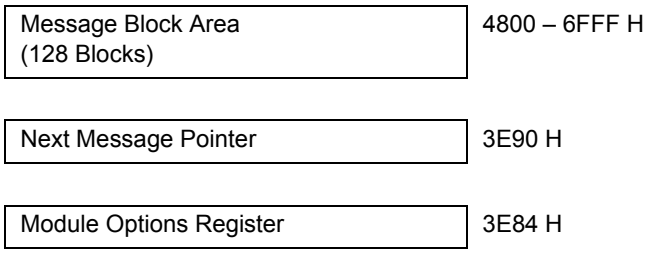


Figure 5-1 Concurrent Monitor Memory Map

5.2 Message Block Area

The message block area is divided into 128 blocks of 80 bytes each. The first block starts at address 4800 H), the second at 4850 (H), the third at 48A0 (H), etc.

Block #127	6FB0 H
•	
•	
•	
Block #2	48A0 H
Block #1	4850 H
Block #0	4800 H

5.2.1 Message Block Structure

Each message block occupies 40 words. These 40 words include a Message Status word, 2 consecutive Time Tag words and all the 1553 message words.

Word 40 is a serial counter. The first message will have a serial counter value of 1; the second message will have a value of 2, etc.

Serial Counter Word
1553 Data Word
•
•
1553 Data Word
1553 Command Word
Time Tag Word #2 (MSB)
Time Tag Word #1 (LSB)
Message Status Word

Concurrent Monitor Message Block Structure

5.2.2 Message Status Word

The Message Status word indicates the status of the message transfer. The module creates this word. Do not confuse it with the 1553 Status word. (See **1553 RT Status Words** on page 2-7.) The contents of the Message Status word are shown below.

Note: The Message Status word is different in RT/Concurrent Monitor mode and BC-RT/Concurrent Monitor mode.

A logic 1 indicates the occurrence of a status flag.

Message Status Word: RT/Concurrent Monitor

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed.
14	**Bus A / B**	Bus on which the message was transferred (1 = BUS A)
13	**Reserved**	Set to 0
12	**Message Error**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status**	A bit other than the Message Error bit in the RT Status word was set. The Error bit is not set in conjunction with this bit.
10	**TX Time Out**	The module, acting as receiver in RT-to-RT message, did not sense a transmitter status word.
09	**Response Error**	Response time error occurred in the message, even if no RT is active on the module.
08	**Invalid Message RT/Concurrent Monitor**	1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT-to-RT message which contains two receive messages.
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity).
06	**Reserved**	Set to 0
05	**Word Count Error**	Incorrect number of words received in the message.
04	**Incorrect RT Address**	Received 1553 Status word did not contain the correct RT address.
03	**Sync Error**	Sync of either the command or the Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**RT2RT Message**	RT-to-RT message was received.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Message Status Word: BC-RT/Concurrent Monitor

Bit	Bit Name	Description
15	**End of Message**	Message transfer completed.
14	**Bus A / B**	Bus on which the message was transferred (1 = BUS A)
13	**Reserved**	Set to 0
12	**Message Error**	Message Error bit (bit 10) in the RT Status word was set.
11	**RT Status**	A bit other than the Message Error bit in the RT Status word was set. The Error bit is not set in conjunction with this bit.
10	**Invalid Message**	1553 message-level error occurred (e.g., Word Count, Sync Error). See other bits set for the exact error. For example: an RT- to-RT message which contains two receive messages.
09	**Response Error**	Response time error occurred in the message, even if no RT is active on the module.
08	**Reserved**	Set to 0
07	**Invalid Word Received**	At least one invalid 1553 word received (i.e. bit count, Manchester code, parity).
06	**Word Count High**	RT transmitted too many words.
05	**Word Count Low**	RT transmitted too few words.
04	**Incorrect RT Address**	Received 1553 Status word did not contain the correct RT address.
03	**Sync Error**	Sync of either the command or the Data Word(s) is incorrect.
02	**Non-Contiguous Data**	Invalid gap between received 1553 words.
01	**RT2RT Message**	RT-to-RT message was received.
00	**Error**	Error occurred. (The error type is defined in one of the other message status bit locations.)

Note: The message contents are valid only after the Message Status word has been written, which is indicated by the End of Message bit being turned on.

5.2.3 1553 Message Words

The 1553 message words are stored in the sequence they appear on the bus, i.e., 1553 Command words, 1553 Status words, 1553 Data Words - all according to the order of the specific type of message.

5.3 Control Register Definitions

5.3.1 Next Message Pointer

Address: 3E90 (H)

The Next Message pointer is a 16-bit pointer that indicates the address of the 1553 message about to be written. The Next Message pointer register is updated at the end of each message storage operation. It cycles from 4800 (H) to 6FB) (H).

5.3.2 Module Options Register

Address: 3E84–3E85 (H)

Read only

The Module Options register is a 16-bit register that identifies the type of on-module firmware.

Bit	Description	
15	Reserved	
14	'1' M4KPx	
10–13	Reserved	
09	'1' 1760	
08	'1' 1553	
00–07	Module Type:	4D H = PMx module 50 H = Px module

Module Options Register

6 Switching Modes of Operation

Many test applications utilizing the *M4K1553Px* simulate only one mode, i.e., Remote Terminal mode. For these applications, the information in this chapter is not relevant.

If your application requires simulation of more than one mode, you can switch from one mode of operation to another, i.e., between the Bus Controller/ Concurrent-RT mode and Remote Terminal modes.

To switch between modes of operation:

1. Halt the operation of the module (via the Start register).
2. Modify the Configuration register to the desired mode.

Hex Value	Operating Mode
02	Remote Terminal
04	BC/Concurrent-RT
08	BM Sequential Fixed-block
10	BM Sequential Link-list
20	BM Look-Up Table

Module Configuration Register Values

3. Set up the memory as required.
4. Set the Start bit in the Start register.

7 Mechanical and Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the *M4K1553Px* module. the following topics are covered:

7.1 Module Layout. 7-1
7.2 LED Indicators. 7-2
7.3 Module Coupling Mode Select DIP switches 7-2
7.4 Connectors 7-3
7.5 Power Requirements. 7-6

7.1 Module Layout

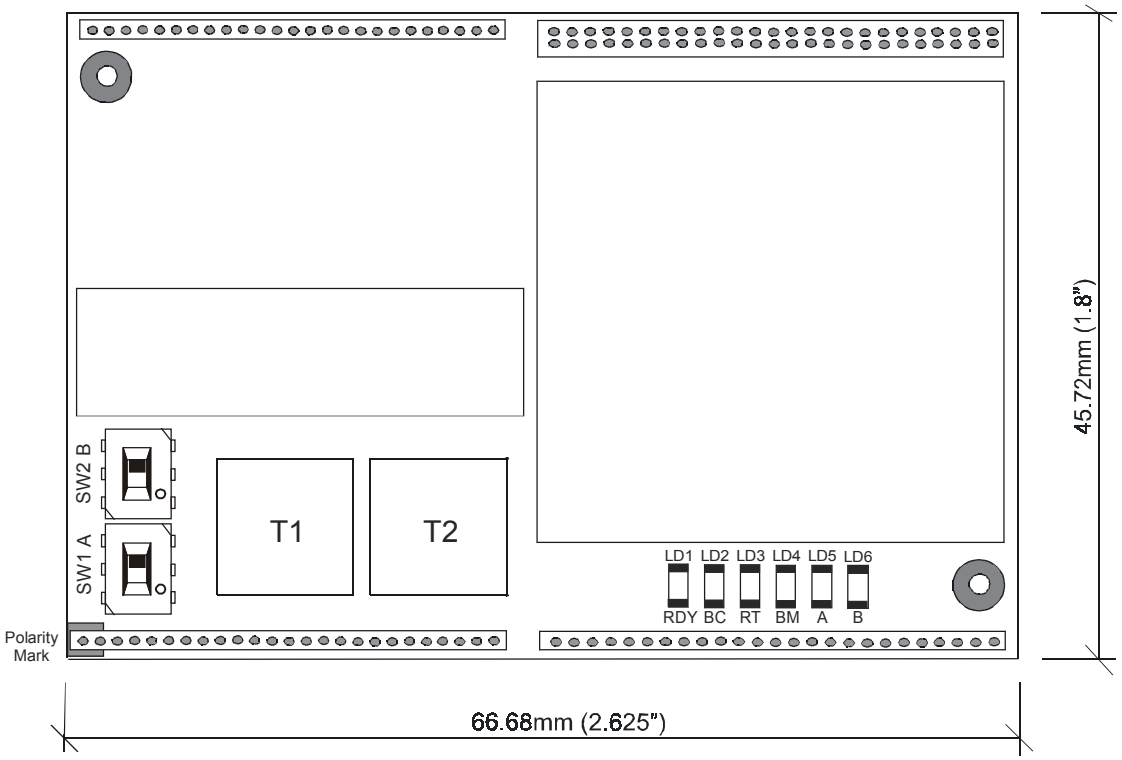


Figure 7-1 *M4K1553Px* Module Layout

7.2 LED Indicators

The *M4K1553Px* module contains six LEDs. The LEDs indicate operational mode and bus activity. The function of each LED is described below.

LED	Indication
LD1	Ready
LD2	BC or BC/RT Mode Active
LD3	RT Mode Active
LD4	Monitor Mode Active
LD5	Bus A Active
LD6	Bus B Active

Led Indicators

7.3 Module Coupling Mode Select DIP switches

The module can be either direct-coupled or transformer-coupled to the 1553 bus. DIP switches are used to select the coupling mode for each bus.

The Table 7-1 defines the DIP switch settings:

Coupling Mode	Switch Position
Direct-Coupled	At the white marker
Transformer-Coupled	Away from the white marker

Table 7-1 DIP Switch Settings Required to Select Coupling Mode

The Table 7-2 defines the DIP switch for each Bus:

Bus	DIP Switch
A	SW1
B	SW2

Table 7-2 Bus DIP Switch

Example: To set Bus A to transformer-coupled, switch SW1 away from the white marker.

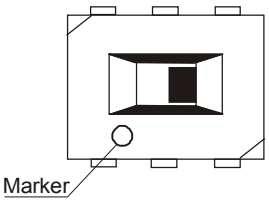


Figure 7-2 DIP Switch: top View

7.3.1 Factory default DIP Switch Settings

The factory default settings are:

DIP Switch	Switch Position	Coupling Mode
SW1 (Bus A)	Away from the white marker	Transformer Coupled
SW2 (Bus B)	Away from the white marker	Transformer Coupled

Table 7-3 Factory Default DIP Switch Settings

7.4 Connectors

Description	Part Number (P/N)
All the I/O communication signals of the M4K1553P*x* module arrive at the **Molex® LFH Female 96-pin connector** located on the EXC-4000 carrier board. Each of the modules on the carrier board is allocated a separate row on the I/O connector	51-26-0000
Molex® 24-pin Terminal Stick	51-25-1012
Four Terminal Sticks inserted into **Plug Connector Sub-assembly**, make up the mating connector for the connector board I/O connector	51-26-0012

Connectors

The *M4K1553Px* module is delivered with a set of all the required connectors. Additional connectors are available directly from Molex®.

7.4.1 Terminal Stick Connector

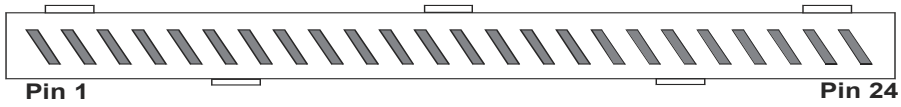


Figure 7-3 Terminal Stick Connector: Front View

7.4.2 Connector Pin Assignments: Px Configuration

Carrier Board Terminal Stick Pin #	Signal Name	Description
1	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
2	BUSALO	Bus A connection Lo
3	BUSAHI	Bus A connection Hi
4 – 9	Not connected	
10	BUSBLO	Bus B connection Lo
11	BUSBHI	Bus B connection Hi
12	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
13 – 22	Not connected	
23	EXSTARTn	External Start TTL input. Provides an option to restart the module externally by applying a pulse of 100 nsec/min. with respect to the GND pin. Before applying the pulse, the module should be fully set up in the required mode, except the Start register bit 00, which should be left at 0. To stop the selected operation, follow the normal procedure described under the Start register.
24	GND	Provides ground reference for the digital signal connections

Px Connector Pin Assignment Configuration

For more information refer to **Ordering Information** in the EXC-4000 carrier board *User's Manual*.

7.4.3 *M4K1553Px* Module Adapter Cable

Excalibur provides a standard adapter cable which converts the Molex® terminal stick to two twinax connectors [P/N: CJ70-49] for Bus A and Bus B.

The twinax connectors mate, for example, with Trompeter PL75 male twinax connectors. These connectors are not supplied by Excalibur.

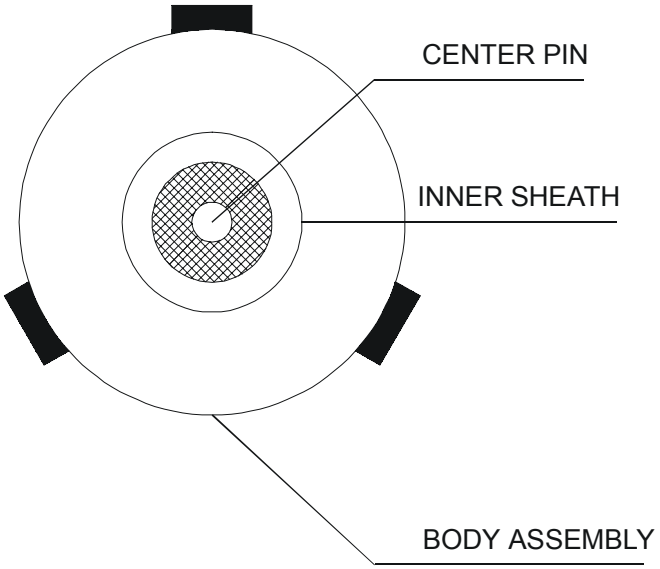


Figure 7-4 CJ70-49 Connector– Front View

7.4.3.1 ADAPTER CABLE CONNECTORS PIN ASSIGNMENTS

	CJ70-49 Pin Position	Signal Name	Description
Bus A	CENTER PIN	BUSHI	Bus A Connection Hi
	INNER SHEATH	BUSLO	Bus A Connection Lo
	BODY ASSEMBLY	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer
Bus B	CENTER PIN	BUSHI	Bus B Connection Hi
	INNER SHEATH	BUSLO	Bus B Connection Lo
	BODY ASSEMBLY	SHIELD	Provided for 1553 cables shield connection. This signal is connected to the case of the computer

Table 7-4 Adapter Cable Connectors Pin Assignments

For more information refer to **Ordering Information** in the EXC-4000 carrier board *User's Manual*.

7.5 Power Requirements

The *M4K1553Px* power requirements are:

+5V @ 420mA (0% duty cycle: non-transmitting on 1553 bus)

+5V @ 480mA (25% duty cycle: transmitting on 1553 bus)

+5V @ 730mA (50% duty cycle: transmitting on 1553 bus)

+5V @ 820mA (75% duty cycle: transmitting on 1553 bus)

+5V @ 1100mA (100% duty cycle: transmitting on 1553 bus)

8 Ordering Information

Chapter 8 explains how to indicate which options you want when ordering a *M4K1553Px* module.

The following suffixes must be added to the name of the module (M4K1553Px) to indicate specific options. The suffixes are added to "M4K1553Px" in the order in which they appear in the table.

Suffix	Description
M	Concurrent Monitor option
-E	Ruggedized, extended temperature operation (-40° – +85°C)
-1760	MIL-STD-1760 options

Part Number	Description
M4K1553Px	MIL-STD-1553 interface module for the Excalibur 4000 family of carrier board. Supports BC, RT BC/Concurrent -RT and BM Modes.
M4K1553Px-E	As above with extended temperature operation (-40° to +85°C)
M4K1553PMx	One MIL-STD-1553 interface module for the Excalibur 4000 family of carrier board. Supports BC, RT BC/Concurrent -RT and BM Modes with an Internal Concurrent Monitor option in RT and BC/RT Modes.
M4K1553Px-1760	MIL-STD-1553 interface module for the Excalibur 4000 family of carrier board. Supports BC, RT BC/Concurrent -RT and BM Modes with MIL-STD-1760 option.

Appendix A MIL-STD-1553 Word Formats

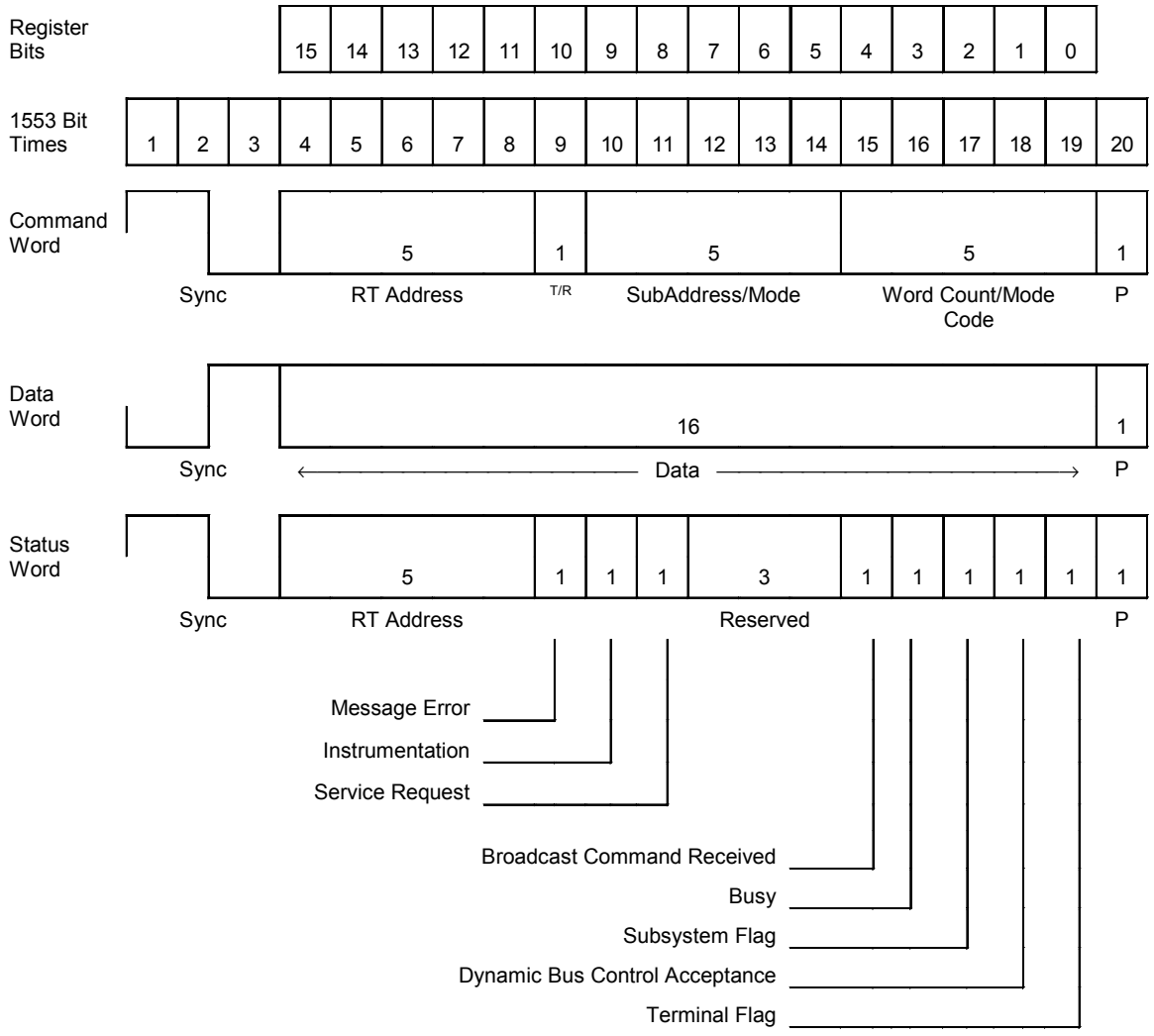


Figure A-1 MIL-STD-1553 Word Formats

Note: T/R = Transmit/Receive
P = Parity

Appendix B MIL-STD-1553 Message Formats

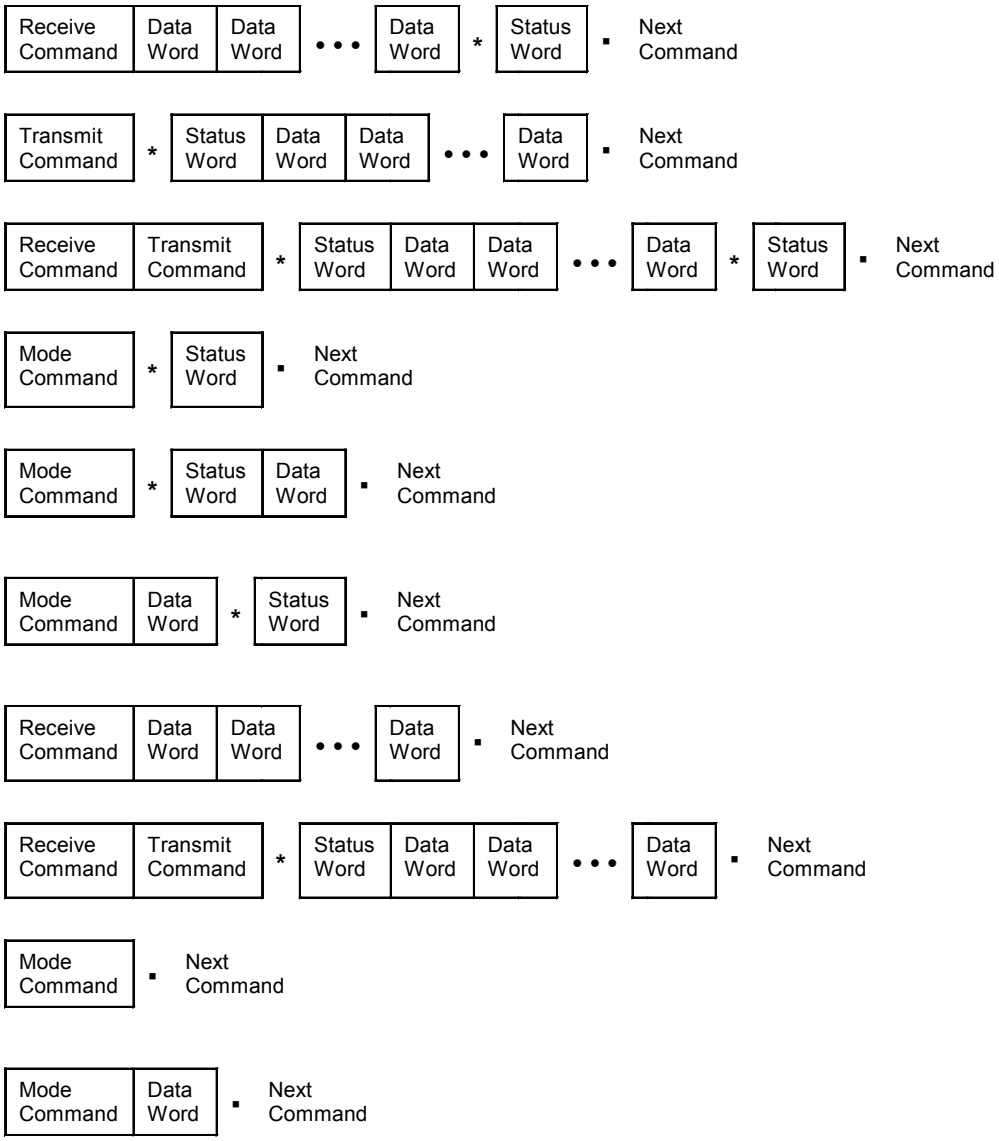


Figure B-1 MIL-STD-1553 Message Formats

Note: * = Response time
▪ = Intermessage Gap

Appendix C Internal Loopback Test

The Internal Loopback Test is used to check the 1553 front-end logic, excluding transceivers and coupling transformers.

To initiate the Internal Loopback Test:

1. Write ED (H) into the Module Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

	Definition	Address in Dual-Port RAM	Status Value
{struct I_LOOPBACK			
usint frame_val;		0	X (not for user)
usint frame_status;	frame time counter status	2	8000H passed, 8001H failed
usint resp_status;	response time counter status	4	8000H passed, 8001H failed
usint early_val;		6	6 LSB must be 15H
usint receive_data1;	first looped word test, using command sync	8	5555H
usint status_1;		A	8000H passed, else failed
usint receive_data2;	second looped word test, using data sync	C	AAAAH
usint status_2;		E	8000H passed, else failed
usint mc_status;	mode code function test	10	8000H passed, else failed
usint ttag_val_lo;		12	30D4H ± 2
usint ttag_val_hi;		14	0
usint ttag_status;	time tag status	16	8000H passed, 8001H failed
usint prl;		18	8 LSB contain the CPU version
} *I_loopback;			

Appendix D External Loopback Test

The External Loopback Test is used to check the 1553 transceivers, transformers and associated bus cables.

Note: The External Loopback Test requires a loopback cable to connect bus A to bus B.

To initiate the External Loopback test:

1. Write FF (H) into the Module Configuration Register.
2. Write 1 into the Start Register.
3. Wait for 0 in the Start Register.

The results of this test are returned to the host in dual-port RAM using the following structure beginning at address 0:

	Definition/conditions for passing E_loopback test [TX-bus, RX-bus, command or data sync]	Address in Dual-Port RAM	Status Value
{struct E_LOOPBACK			
usint frame_val;		0	X (not for user)
usint frame_status;	frame time counter status	2	8000H passed, 8001H failed
usint cmd_send[8];		4	cmd_send[0]: 5555H
	TX-A, RX-A, command sync	6	cmd_send[1]:8000H passed, else failed
		8	cmd_send[2]: 1234H
	TX-A, RX-B data sync	A	cmd_send[3]:8000H passed, else failed
		C	cmd_send[4]: 5555H
	TX-B, RX-A command sync	E	cmd_send[5]:8000H passed, else failed
		10	cmd_send[6]: 1234H
	TX-B, RX-B data sync	12	cmd_send[7]:8000H passed, else failed
usint ttag_val_lo		14	30D4H ± 2
usint ttag_val_hi		16	0
usint ttag_status;	time tag status	18	8000H passed, 8001H failed
} *E_loopback;			

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